Sapphire Stream Technology

SST SQC6490 SOM

Datasheet

Rev. V1.1.2
July 15, 2025

DN: sst-x3-13111.2

Revision History

Revision	Date	Author	Description
1.0	June 27, 2023	Qiming Duan	Initial release.
1.0.1	Aug 30, 2023	Qiming Duan	• Update 1.6. Module laser marking. • Update 1.7. SMT assembly guide. • Fix format problems.
1.0.2	Sep 01, 2023	Qiming Duan	• Update Figure 1-5. • Add Table 1-4.
1.0.3	Jan 16, 2024	Shengxiong He	• Update Figure 1-1. • Update the introductary paragraph in Chapter 2. Interface Specifications. • Update all the pin numbers in Table 2-5. • Add info. of PM7250B in Table 2-17. • Update info. of Y22, Y23, AA22, AA23, AB22, AB23, AC22, AC23, AE25, AD27, AA24, AA25, AA26, AA27, D22, F23, AC29, B21, AE27, AF30, AF27, E2, E1, E3, AG29, D1, AB30, AG28, AF29, AE28, AE26, and AB25 in Table 2-20. • Update info. of VREG_L2C_1P8 and VREG_L2B_3P072 in Table 3-3. • Add content to the following chapter/sections: ▫ 3.14. Power consumption ▫ 3.15. Thermal ▫ Chapter 4. Packaging
1.1	Mar 20, 2024	Tianyang Li	• Update Figure 1-1, Figure 2-1, and Figure 1-5. • Update DSI relevant information in Table 1-1. • Update description of PX_2 in Table 2-1. • Change the note of M24 in Table 2-20 to NC. • Add default value of VDDPX_3 in 3.4. Digital-logic characteristics. • Update 3.4.2. SD card digital I/O characteristics.
1.1.1	Feb 21, 2025	Tianyang Li	Update Table 2-20.
1.1.2	July 15, 2025	Qiming Duan	• Update the following tables: ▫ Table 3-2 ▫ Table 3-6 ▫ Table 3-7 ▫ Table 3-8 ▫ Table 3-9 ▫ Table 3-10 ▫ Table 3-11 ▫ Table 3-12 ▫ Table 3-13 ▫ Table 3-15 • Update Figure 4-1.

Table List

About This Document

- Illustrations in this documentation might look different from your product.
- Depending on the model, some optional accessories, features, and software programs might not be available on your device.
- Depending on the version of operating systems and programs, some user interface instructions might not be applicable to your device.
- Documentation content is subject to change without notice. SST makes constant improvements on the documentation of your computer, including this guidebook.

Table of Contents

Chapter 1. Introduction

SST SQC6490 SOM (System on Module) is integrated with Qualcomm® QCS6490 SoC, a 6 nm processor with superior performance, power efficiency, and powerful computing (12.5 TOPS). It supports 4K@60FPS video decoding and 4K@30FPS video encoding, five MIPI CSIs, as well as a rich set of peripheral interfaces, including GPIO, UART, I2C, I3C, SPI, USB 3.1 and PCIe. SQC6490 SOM is a high performance AIoT SOM for building handheld devices, industrial robots, service robots, rugged tablet and edge computing, providing customers with hardware interfaces and software SDK to validate functions and build the prototype quickly.

1.1. Key features

The following table shows the detailed features of QCS6490 and SQC6490 SOM.

Table 1-1.Key features and performance of QCS6490

Item	Description
Applications Processor	Qualcomm® Kryo™ CPU 670 built on Arm v8 Cortex technology • Kryo Gold plus: High-performance core up to 2.7 GHz • Kryo Gold: Three high-performance cores at 2.4 GHz • Kryo Silver: Four low-power cores at 1.9 GHz
Digital signal processing and AI	Compute Hexagon DSP with dual HVX and Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator • Used for video playback enhancements, virtual reality, computer vision, camera snapshot enhancements, video capture enhancement, machine learning, etc. • The Hexagon CP is a vision and imaging hardware accelerator to offload and accelerate the Hexagon software algorithmic functions.
Adreno GPU (Graphic Processing Unit)	• Adreno GPU 643 • OpenGL ES 3.2, Vulkan 1.x • OpenCL 2.0, DX FL12
Adreno VPU (Video Processing Unit)	Adreno VPU 633 – fifth-generation UHD video processing unit • Video decode: Up to 4K@60FPS for H.264/H.265/VP9 • Video encode: Up to 4K@30FPS for H.264/H.265 • Video concurrency: 1080P@60FPS decode and 1080P@60FPS encode/4K@30FPS decode + 1080P@30FPS encode • HDR playback: Support for HDR10 and HDR10+ • HFR capture: 720P@480FPS or 1080P@240FPS
Display support	Adreno DPU 1075: • Maximum resolution for internal panel: FHD+ 144 Hz QCLTM, HDR10+, WCG, improved inline rot, rounded corner, SPR, Demura, CWB-ROI • One 4-lane DSI D-PHY 1.2 or C-PHY 1.2 up to 4K@30FPS; VESA DSC 1.2 • 4K@60FPS display support over DisplayPort (USB3 + DisplayPort concurrency)

Item	Description
Camera support	Qualcomm Spectra 570L: 36 + 22 MP at 30 fps/3x22 MP 30 fps ZSL Qualcomm Spectra 570L ISP supports connectivity to multiple cameras due to five C-PHY/D-PHY interfaces. • Real-time sensor input resolution: 22 + 22 + 22 • Three IFE + two IFE lite, five concurrent MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 configuration • 5 x D-PHY v1.2/C-PHY v1.2
Connectivity	• Qualcomm universal peripheral (QUP) ports: 21 multiplexed serial interface functions • USB: 1 x USB 3.1 port: Gen 1, 5 Gbps (DisplayPort + data), support Type-C with DisplayPort v1.4 and 1 x USB 2.0 HS port • PCIe: 2 x PCIe Gen 3 (1-lane, 2-lane) • Secure digital interfaces: 2 x SDC

Table 1-2.Key features and performance of SQC6490 SOM

Item	Description
Platform	Dragonwing™ QCS6490 Qualcomm® Kryo™ CPU 670 • Kryo Gold plus: High-performance core up to 2.7 GHz • Kryo Gold: Three high-performance cores at 2.4 GHz • Kryo Silver: Four low-power cores at 1.9 GHz Qualcomm® Adreno™ GPU 643, Adreno 633 VPU, Adreno DPU 1075 Qualcomm® Compute Hexagon™ DSP with dual HVX, Hexagon Co-processor (Hexagon CP) 2.0 and Hexagon Tensor Accelerator Qualcomm® Spectra™ 570L image processing
Memory [1)]	LPDDR4× 8GB + UFS2.x 128GB, uMCP
Video Encode	4K@30FPS for H.264/H.265
Video Decode	4K@60FPS for H.264/H.265/VP9
Display interfaces	1x MIPI-DSI 4-lane; FHD+ (1080x2520) 8L @144FPS
Camera Interfaces	5 x 4-lane MIPI CSI D-PHY (2 of them compatible to support C-PHY)
Peripherals	1 x USB 3.1 with DP, 1 x USB2.0, 2x PCIe Gen 3 (1-lane, 2-lane), 2 x SoundWire, 2 x SDC (4-bit), 3 x DMIC interface, GPIOs, QUPs (UART/I2C/SPI)
Operating Environment	Operating Temperature: -35°C ~ 75°C [#]
Form Factor	LGA
Certification	RoHS*/REACH*
Voltage	3.4V~4.5V
Dimensions	39mm x 33mm x 2.75mm (excluding height of the bottom shielding case)
Operating System	Android 13 & Ubuntu LE (Planning)

[1)] Please note that storage devices such as UFS, eMMC, NAND, etc. have a limit to the total amount of data that can be written. Exceeding this limit can cause damage to the storage device.

[#] The SOM operation temperature shall not exceed relevant IC temperature scope.

[*] Planning.

1.2. Hardware block diagram

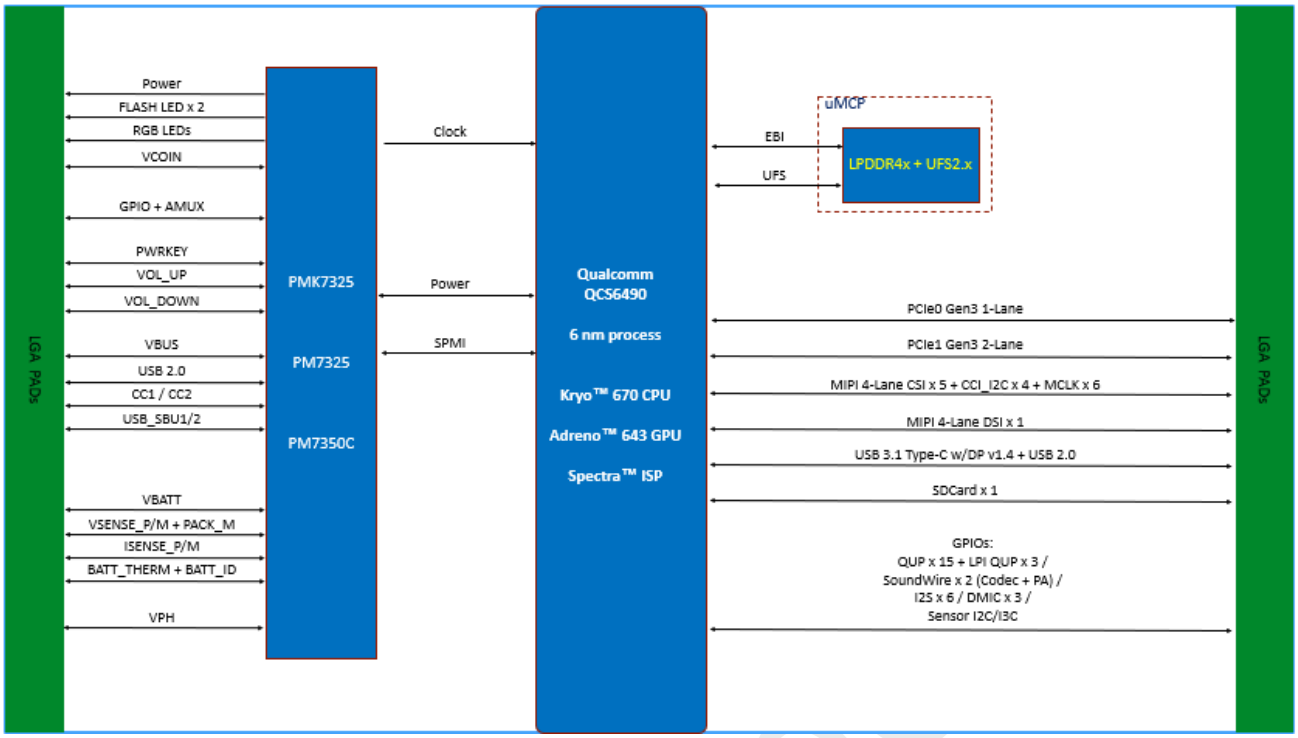

Figure 1-1.SQC6490 SOM Hardware Block Diagram

1.3. Mechanical size

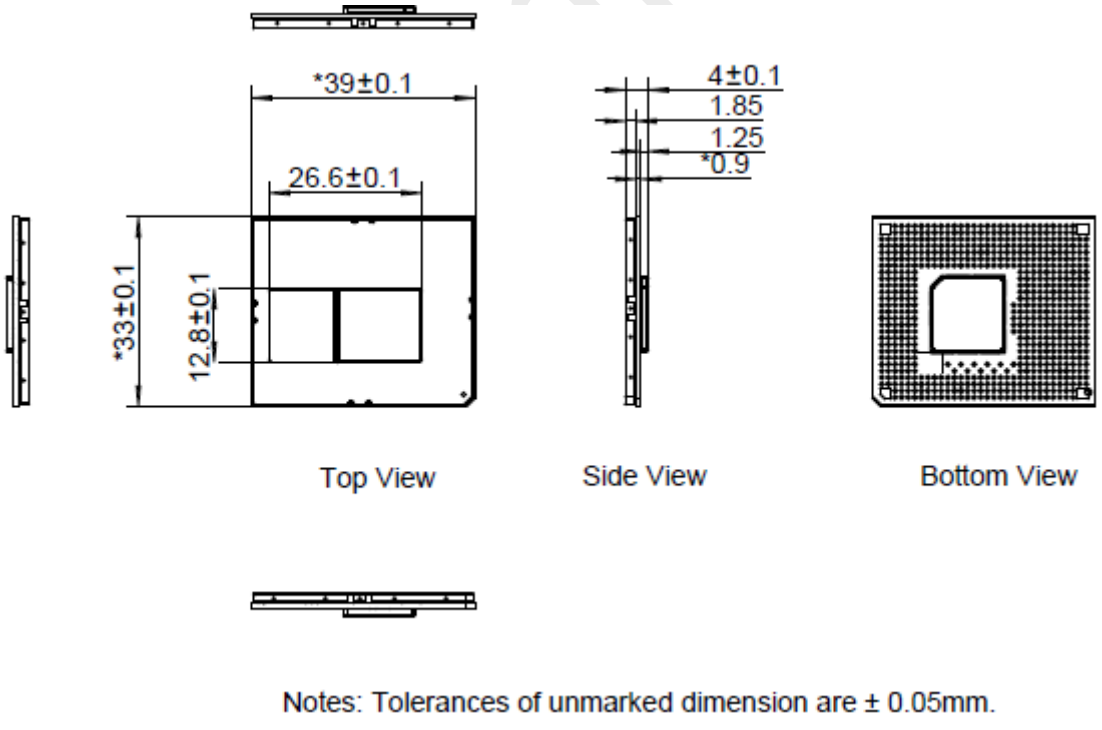

Figure 1-2.SQC6490 SOM Mechanical Dimensions

1.4. Package dimensions

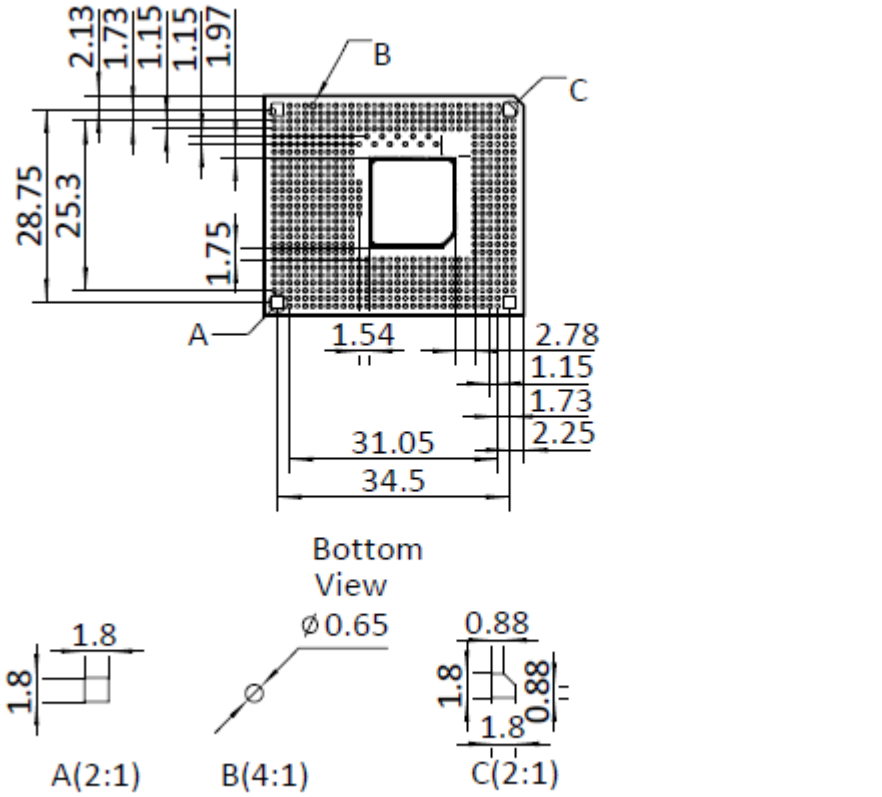

Figure 1-3.SQC6490 SOM Package Dimensions

1.5. Stencil design and aperture

To supply sufficient soldering paste and keep reliable soldering joints, add the thickness of stencil partly on the top surface. The stencil aperture for single sheet cannot be greater than 3.0mm×4.0mm and the exceeded part should be divided into smaller apertures with applicable shelves. A clearance of over 2.0mm should be kept between the outward end of the aperture and the component if there are components around the module.

➲ **NOTES**:

- For the convenience of heating and repairing, it is recommended that no components should be placed in the area at the backside of the module on PCB.
- In order to avoid reverse polarity of the module, it is recommended to use asymmetric pads at the bottom of the module to identify the module polarity during module placement.
- It is not recommended to add any silkscreen in the area where the module is mounted to avoid the height that may influence the solder paste printing and soldering quality.
- When there is a need to step-up the stencil, all 01005/0201, 0.4mm-pitch and 0.5mm-pitch components should be kept over 5.0mm away from the stepped-up area to avoid solder bridging that is caused by thicker solder paste.

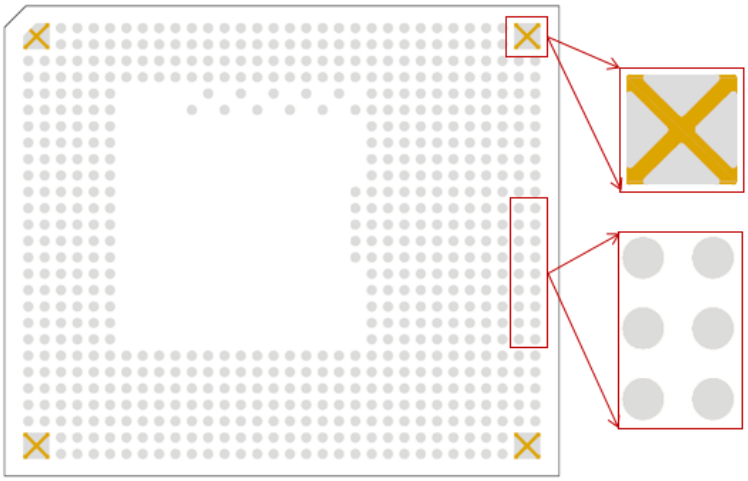

Figure 1-4.Stencil Aperture Diagram

Requirement description

- **Stencil thickness**

  Area of the module should be partly stepped-up to 0.15mm-0.18mm.

  ➲ **NOTE:** Ignore this requirement if the bottom of the module has pre-planted solder paste or solder ball.

- **Circular pads**

  The aperture for each single pad should be centered with area increased to 110%~120% if necessary (see Figure 1-4).

- **Pads at four corners**

  The stencil aperture should be designed with 60%~65% area of the corresponding pad (see Figure 1-4).

1.6. Module laser marking

Refer to Figure 1-6 for the module laser marking of SST SQC6490.

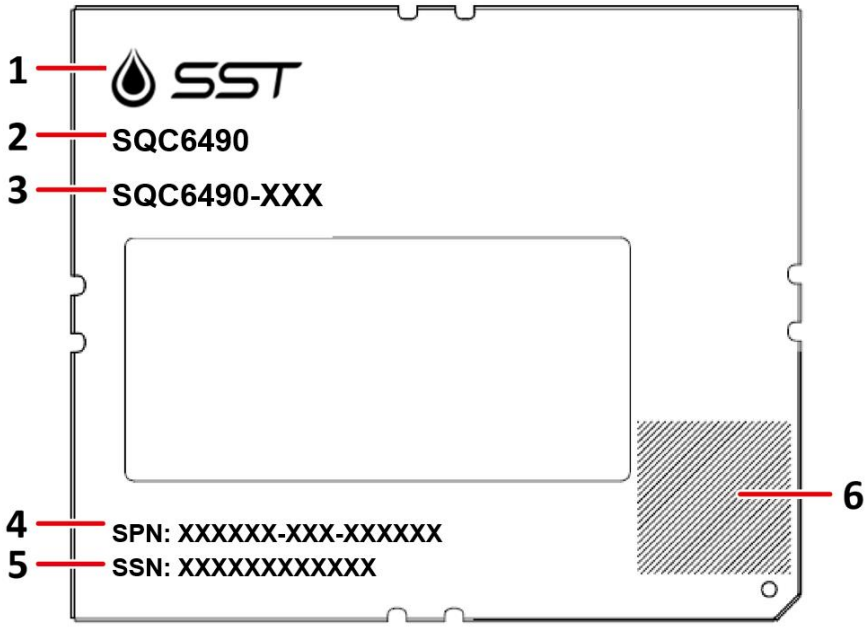

Figure 1-5.Laser Marking of SQC6490 SOM

Table 1-3.Module laser marking description

1. Company name/logo	4. Part number
2. Product name	5. Serial number
3. PCBA version	6. QR code

➲ **NOTES**:

- Figure 1-5 is for reference only and may vary with the specific module.
- The part number may be updated. Please confirm with the supplier about the accurate information.

Table 1-4.SST SQC6490 configuration

SOM	Model Name	Memory	SPN (SST Product No.)
SQC6490	SQC6490P-U8A	8GB+128GB	SQC6490P-U8A-3690000

1.7. SMT assembly guide

To reduce module trial cost and improve project implementation efficiency, it is **strongly recommended** to comprehend the Common SMT Assembly Guidelines and the LCC/LGA Module Carrier Board Design Guidelines for DFM before the early stage of module layout design.

Additionally, if necessary, you can contact us at service@sapphirestreamtech.com for assistance in review of PCBA placement design.

Chapter 2. Interface Specifications

This chapter introduces definitions of all the interfaces to facilitate design and verification on SST SQC6490 SOM.

For information on high-speed signals (including but not limited to MIPI CSI, MIPI DSI, PCIe, SDC, etc.), please contact OUR FAE team (service@sapphirestreamtech.com).

2.1. Interface parameter definition

Table 2-1. Interfaces parameter definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DI	Digital input (CMOS)
DSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DO	Digital output (CMOS)
H	High-voltage tolerant
Z	High-impedance (Hi-Z) output
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
PX_0	Power group 0, it is 1.8V.
PX_2	SDC Power group 2, it is 1.8V or 2.96V.
PX_3	Power group 3, it is 1.8V.
PX_7	Power group 7, it is 1.8V.
MV	Medium voltage
LV	Low voltage

2.2. Interface detailed description

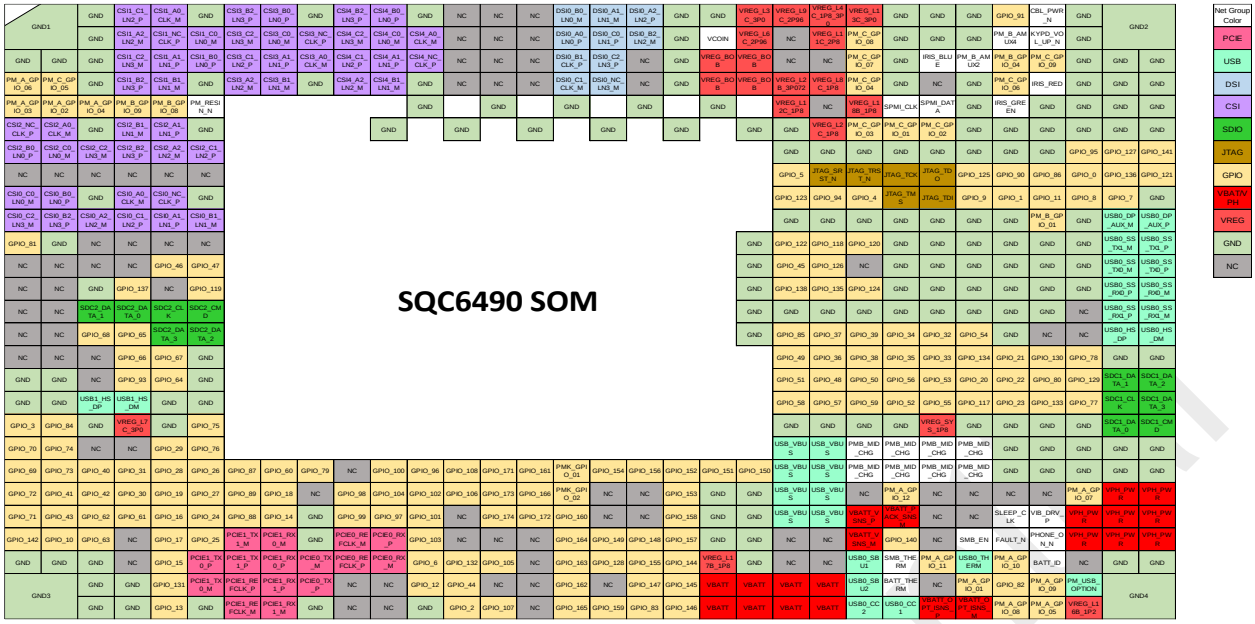

Figure 2-1. SQC6490 SOM Pin Location

2.2.1. Power supply interface

Table 2-2 describes all interfaces of SOM power supply.

For the detailed parameter request, refer to Chapter 3. Electrical Characteristics.

Table 2-2. Power supply definition

Pin name	Pin	Type	Description, V_typ@I_rated
VBATT	AF20,AF21,AF22,AF23, AG20,AG21,AG22,AG23	PI,PO	Power supply input for SOM (3.8V typical)
VPH_PWR	AB31,AB32,AC30,AC31, AC32,AD30,AD31,AD32	PO	Primary system supply node
USB_VBUS	Y22,Y23,AA22,AA23,AB22, AB23,AC22,AC23	PO,PI	
VCOIN	B20	PI,PO	Coin-cell charge and supply recommend to use 22uF x 3 for VCOIN
VREG_BOB	C20,C21,D20,D21	PO	Buck-boost output 3.3V@1A (will increase to 3.6V during bootup of the SOM)
VREG_L16B_1P2	AG30	PO	1.2V~1.3V, 1.2V typ
VREG_L17B_1P8	AE20	PO	1.8V~1.9V, 1.8V typ WCD_VDD_BUCK by default
VREG_L18B_1P8	E24	PO	1.8V~2.0V, 1.8V typ (PX_3) Just used for GPIO pull-up
VREG_L2B_3P072	D22	PO	3.072V typ; USB redriver by default
VREG_L3C_3P0	A21	PO	2.7V~3.54V, 3V typ; Touch screen by default

Pin name	Pin	Type	Description, V_typ@I_rated
VREG_L4C_1P8_3P0	A23	PO	1.62V~3.3V, 1.8V typ; UIM1 Power Supply
VREG_L2C_1P8	F23	PO	1.62V~1.98V, 1.8V typ; MEMS_DMIC_VDD by default
VREG_L7C_3P0	W4	PO	3.0V~3.54V, 3V typ; Sensors by default
VREG_L8C_1P8	D23	PO	1.62V~2V, 1.8V typ; Sensors by default
VREG_L11C_2P8	B23	PO	1.65V~3.54V, 2.8V typ Connectivity by default
VREG_L12C_1P8	E22	PO	1.62V~1.98V, 1.8V typ; OLED VDDIO by default
VREG_L13C_3P0	A24	PO	2.7V~3.54V, 2.8V typ; OLED VCI by default
VREG_SYS_1P8	W26	PO	System 1.8 V I/O output. Reserved for debug; leave it floating.
GND	GND1,GND2,GND3,GND4,A3, A6,A9,A12,A19,A20,A25,A26, A27,A30,B3,B19,B25,B26, B27,B30,C1,C2,C3,C19,C25, C30,C31,C32,D3,D6,D9,D12, D19,D25,D27,D30,D31,D32, E12,E14,E16,E18,E20,E27, E29,E30,E31,E32,F3,F6,F11, F13,F15,F17,F19,F21,F22,F27, F28,F29,F30,F31,F32,G22, G23,G24,G25,G26,G27,G28, G29,J3,J6,J32,K22,K23,K24, K25,K26,K27,K28,K30,L2,L21, L25,L26,L27,L28,L29,L30, M21,M25,M26,M27,M28, M29,M30,N3,N21,N25,N26, N27,N28,N29,N30,P21,P22, P23,P24,P25,P26,P27,P28, P29,R21,R28,T6,T31,T32,U1, U2,U6,V1,V2,V5,V6,W3,W5, W22,W23,W24,W25,W27, W28,W29,W30,Y28,Y29,Y30, Y31,Y32,AA28,AA29,AA30, AA31,AA32,AB20,AB21,AC9, AC20,AC21,AD9,AD20,AD21, AE1,AE2,AE3,AE21,AE31, AE32,AF3,AF4,AG3,AG4,AG6, AG9,AG12	GND	GND

2.2.2. Camera interfaces

The SOM supports 5x 4-lane camera interfaces.

Table 2-3. Camera interface definition

Pin name	Pin	Volt.	Type	Decription	Notes
CSI0_NC_CLK_P	J5	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – positive	MIPI signals of Camera0
CSI0_A0_CLK_M	J4	CSI	AI	MIPI CSI 0 (D-PHY), differential clock – negative	
CSI0_B0_LN0_P	J2	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – positive	
CSI0_C0_LN0_M	J1	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 0 – negative	
CSI0_A1_LN1_P	K5	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – positive	
CSI0_B1_LN1_M	K6	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 1 – negative	
CSI0_C1_LN2_P	K4	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – positive	
CSI0_A2_LN2_M	K3	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 2 – negative	
CSI0_B2_LN3_P	K2	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 3 – positive	
CSI0_C2_LN3_M	K1	CSI	AI	MIPI CSI 0 (D-PHY), differential lane 3 – negative	
CSI1_NC_CLK_P	B5	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect	MIPI signals of Camera1 (Support C-PHY)
CSI1_A0_CLK_M	A5	CSI	AI	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A	
CSI1_B0_LN0_P	C6	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – positive MIPI CSI 1 (C-PHY), trio lane 0 – B	
CSI1_C0_LN0_M	B6	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C	
CSI1_A1_LN1_P	C5	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A	
CSI1_B1_LN1_M	D5	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B	
CSI1_C1_LN2_P	A4	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C	
CSI1_A2_LN2_M	B4	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A	
CSI1_B2_LN3_P	D4	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3 – positive MIPI CSI 1 (C-PHY), trio lane 2 – B	
CSI1_C2_LN3_M	C4	CSI	AI	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C	
CSI2_NC_CLK_P	F1	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – positive	MIPI signals of Camera2
CSI2_A0_CLK_M	F2	CSI	AI	MIPI CSI 2 (D-PHY), differential clock – negative	
CSI2_B0_LN0_P	G1	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – positive	
CSI2_C0_LN0_M	G2	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 0 – negative	
CSI2_A1_LN1_P	F5	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – positive	
CSI2_B1_LN1_M	F4	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 1 – negative	
CSI2_C1_LN2_P	G6	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – positive	
CSI2_A2_LN2_M	G5	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 2 – negative	
CSI2_B2_LN3_P	G4	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3 – positive	
CSI2_C2_LN3_M	G3	CSI	AI	MIPI CSI 2 (D-PHY), differential lane 3 – negative	

Pin name	Pin	Volt.	Type	Decription	Notes
CSI3_NC_CLK_P	B9	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), no connect	MIPI signals of Camera3 (Support C-PHY)
CSI3_A0_CLK_M	C9	CSI	AI	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A	
CSI3_B0_LN0_P	A8	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B	
CSI3_C0_LN0_M	B8	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C	
CSI3_A1_LN1_P	C8	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – positive MIPI CSI 3 (C-PHY), trio lane 1 – A	
CSI3_B1_LN1_M	D8	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B	
CSI3_C1_LN2_P	C7	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C	
CSI3_A2_LN2_M	D7	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A	
CSI3_B2_LN3_P	A7	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3 – positive MIPI CSI 3 (C-PHY), trio lane 2 – B	
CSI3_C2_LN3_M	B7	CSI	AI	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C	
CSI4_NC_CLK_P	C12	CSI	AI	MIPI CSI 4 (D-PHY), differential clock – positive	MIPI signals of Camera4
CSI4_A0_CLK_M	B12	CSI	AI	MIPI CSI 4 (D-PHY), differential clock – negative	
CSI4_B0_LN0_P	A11	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 0 – positive	
CSI4_C0_LN0_M	B11	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 0 – negative	
CSI4_A1_LN1_P	C11	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 1 – positive	
CSI4_B1_LN1_M	D11	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 1 – negative	
CSI4_C1_LN2_P	C10	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 2 – positive	
CSI4_A2_LN2_M	D10	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 2 – negative	
CSI4_B2_LN3_P	A10	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 3 – positive	
CSI4_C2_LN3_M	B10	CSI	AI	MIPI CSI 4 (D-PHY), differential lane 3 – negative	
CCI_I2C0_SDA/GPIO_69	AA1	PX_3	B	Dedicated camera control interface I²C 0 serial data	Requires an external pull-up resistor
CCI_I2C0_SCL/GPIO_70	Y1	PX_3	DO	Dedicated camera control interface I²C 0 clock	
CCI_I2C1_SDA/GPIO_71	AC1	PX_3	B	Dedicated camera control interface I²C 1 serial data	
CCI_I2C1_SCL/GPIO_72	AB1	PX_3	DO	Dedicated camera control interface I²C 1 clock	
CCI_I2C2_SDA/GPIO_73	AA2	PX_3	B	Dedicated camera control interface I²C 2 serial data	
CCI_I2C2_SCL/GPIO_74	Y2	PX_3	DO	Dedicated camera control interface I²C 2 clock	
CCI_I2C3_SDA/GPIO_75	W6	PX_3	B	Dedicated camera control interface I²C 3 serial data	
CCI_I2C3_SCL/GPIO_76	Y6	PX_3	DO	Dedicated camera control interface I²C 3 clock	
CAM_MCLK0/GPIO_64	U5	PX_3	DO	Camera master clock 0	
CAM_MCLK1/GPIO_65	R4	PX_3	DO	Camera master clock 1	
CAM_MCLK2/GPIO_66	T4	PX_3	DO	Camera master clock 2	

Pin name	Pin	Volt.	Type	Decription	Notes
CAM_MCLK3/GPIO_67	T5	PX_3	DO	Camera master clock 3	
CAM_MCLK4/GPIO_68	R3	PX_3	DO	Camera master clock 4	
CAM_MCLK5/GPIO_93	U4	PX_3	DO	Camera master clock 5	

2.2.3. Display interface

The SOM supports 1x 4-lane MIPI_DSI interfaces.

Table 2-4. Display interfaces definition

Pin name	Pin	Volt.	Typ	Description	Notes
DSI0_B1_CLK_P	C16	DSI	AO	MIPI DSI 0 (D-PHY), differential clock – positive	MIPI signals for MIPI LCM. Compliant with MIPI Alliance Specification for Display Serial Interface.
DSI0_C1_CLK_M	D16	DSI	AO	MIPI DSI 0 (D-PHY), differential clock – negative	
DSI0_A0_LN0_P	B16	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 0 – positive	
DSI0_B0_LN0_M	A16	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 0 – negative	
DSI0_C0_LN1_P	B17	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 1 – positive	
DSI0_A1_LN1_M	A17	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 1 – negative	
DSI0_A2_LN2_P	A18	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 2 – positive	
DSI0_B2_LN2_M	B18	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 2 – negative	
DSI0_C2_LN3_P	C17	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 3– positive	
DSI0_NC_LN3_M	D17	DSI	AO	MIPI DSI 0 (D-PHY), differential lane 3 – negative	

2.2.4. Touchscreen interface

Touchscreen panels are supported using I2C buses and GPIOs configured as discrete digital inputs.

Table 2-5. Touchscreen interfaces definition

Pin name	Pin	Voltage	Type	Description
GPIO_52	V25	PX_3	B	TP0_SDA
GPIO_53	U26	PX_3	DO	TP0_SCL
GPIO_81	L1	PX_3	DI	TP0_INT
GPIO_105	AE14	PX_3	DO	TP0_RST

2.2.5. Audio interface

The SOM provides SoundWire, DMIC and I2S interfaces for audio. SoundWire interface is special for external codec IC, which can build audio functions of the systeme. DMIC interface can be used to directly connect up to 6 PDM MICs.

Table 2-6. Audio interface definition

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_144	AE19	PX_3	DO	SoundWire transmit clock	SoundWire transmit
GPIO_145	AF19	PX_3	DO	SoundWire transmit data 0	
GPIO_146	AG19	PX_3	DO	SoundWire transmit data 1	
GPIO_158	AC19	PX_3	DO	SoundWire transmit data 2	
GPIO_147	AF18	PX_3	DI	SoundWire receive clock	SoundWire receive
GPIO_148	AD18	PX_3	DI	SoundWire receive data 0	
GPIO_149	AD17	PX_3	DI	SoundWire receive data 1	
GPIO_154	AA17	PX_3	DO	SoundWire clock for WSA	AUDIO PA SoundWire
GPIO_155	AE18	PX_3	B	SoundWire data for WSA	
GPIO_150	AA21	PX_3	DO	LPI DMIC 1 Clock	DMIC I/F
GPIO_151	AA20	PX_3	DI	LPI DMIC 1 Data	
GPIO_152	AA19	PX_3	DO	LPI DMIC 2 clock	
GPIO_153	AB19	PX_3	DI	LPI DMIC 2 data	
GPIO_156	AA18	PX_3	DO	LPI DMIC 3 clock	
GPIO_157	AD19	PX_3	DI	LPI DMIC 3 data	
GPIO_96	AA12	PX_3	DO	Primary MI²S master clock	Primary MI²S master clock
GPIO_97	AC11	PX_3	DO	MI²S 0 clock	MI2S0
GPIO_98	AB10	PX_3	B	MI²S 0 serial data channel 0	
GPIO_99	AC10	PX_3	B	MI²S 0 serial data channel 1	
GPIO_100	AA11	PX_3	B	MI²S 0 serial data word select	
GPIO_101	AC12	PX_3	B	MI²S 2 clock	MI2S2
GPIO_102	AB12	PX_3	B	MI²S 2 serial data channel 0	
GPIO_103	AD12	PX_3	B	MI²S 2 serial data word select	
GPIO_104	AB11	PX_3	B	MI²S 2 serial data channel 1	
GPIO_105	AE14	PX_3	DO B	Secondary MI²S master clock MI²S 1 serial data channel 1	MI2S1
GPIO_106	AB13	PX_3	B	MI²S 1 clock	
GPIO_107	AG14	PX_3	B	MI²S 1 serial data channel 0	
GPIO_108	AA13	PX_3	B	MI²S 1 serial word select	
GPIO_144	AE19	PX_3	B	LPI quaternary MI²S clock	LPI MI2S 4 bit
GPIO_145	AF19	PX_3	B	LPI quaternary MI²S word select	
GPIO_146	AG19	PX_3	B	LPI quaternary MI²S data 0	
GPIO_147	AF18	PX_3	B	LPI quaternary MI²S data 1	
GPIO_148	AD18	PX_3	B	LPI quaternary MI²S data 2	

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_149	AD17	PX_3	B	LPI quaternary MI²S data 3	
GPIO_150	AA21	PX_3	B	LPI I2S 1 clock	LPI I2S1
GPIO_151	AA20	PX_3	B	LPI I2S 1 word select	
GPIO_152	AA19	PX_3	B	LPI I2S 1 Data 0	
GPIO_153	AB19	PX_3	B	LPI I2S 1 Data 1	
GPIO_154	AA17	PX_3	B	LPI MI²S 2 clock	LPI I2S2
GPIO_155	AE18	PX_3	B	LPI I2S 2 Word select	
GPIO_156	AA18	PX_3	B	LPI I2S 2 Data 0	
GPIO_157	AD19	PX_3	B	LPI I2S 2 data 1	

2.2.6. USB & DisplayPort interface

The SOM supports 1x USB 3.1 GEN1, with Type-C with DisplayPort and 1x USB2.0.

Table 2-7. USB &DP interface definition

Pin name	Pin	Type	Description	Notes
USB_SS-H_HS-L_SEL	AD25	DI	Connected to ID Pin of Micro USB. Not supported on SOM by default.	Keep floating.
USB0_CC1	AG25	AI, PO	CC1 Pin for the USB Type-C connector or OTG mode enable	
USB0_CC2	AG24	AI, PO	CC2 Pin for the USB Type-C connector	
USB0_SBU1	AE24	DI	Type-C side band signal SBU1; protected to 22 V max.	
USB0_SBU2	AF24	DO	Type-C side band signal SBU2; protected to 22 V max.	
USB0_DP_AUX_P	K32	AI, AO	DisplayPort auxiliary channel – positive	Native DP
USB0_DP_AUX_M	K31	AI, AO	DisplayPort auxiliary channel – negative	
USB0_HS_DP	R31	AI, AO	USB 2.0 high-speed data – positive	
USB0_HS_DM	R32	AI, AO	USB 2.0 high-speed data – negative	
USB0_SS_TX0_P	M32	AO	USB 3.0 Type C PHY transmit 0 – positive	
USB0_SS_TX0_M	M31	AO	USB 3.0 Type C PHY transmit 0 – negative	
USB0_SS_RX0_P	N31	AI	USB 3.0 Type C PHY receiver 0 – positive	
USB0_SS_RX0_M	N32	AI	USB 3.0 Type C PHY receiver 0 – negative	
USB0_SS_TX1_P	L32	AO	USB 3.0 Type C PHY transmit 1 – positive	
USB0_SS_TX1_M	L31	AO	USB 3.0 Type C PHY transmit 1 – negative	
USB0_SS_RX1_P	P31	AI	USB 3.0 Type C PHY receiver 1 – positive	
USB0_SS_RX1_M	P32	AI	USB 3.0 Type C PHY receiver 1 – negative	
USB1_HS_DP	V3	AI, AO	USB1_HS – positive	USB1 2.0
USB1_HS_DM	V4	AI, AO	USB1_HS – negative	

2.2.7. PCIe interface

The SOM supports two Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

Table 2-8. PCIe interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PCIe0_REFCLK_P	AE10	–	AI, AO	PCIe 0 Gen 3 reference clock – positive	PCIe0 1-lane
PCIe0_REFCLK_M	AD10	–	AI, AO	PCIe 0 Gen 3 reference clock – negative	
PCIe0_TX_P	AF9	–	AO	PCIe 0 Gen 3 transmit – positive	
PCIe0_TX_M	AE9	–	AO	PCIe 0 Gen 3 transmit – negative	
PCIe0_RX_P	AD11	–	AI	PCIe 0 Gen 3 receive – positive	
PCIe0_RX_M	AE11	–	AI	PCIe 0 Gen 3 receive – negative	
PCIe0_CLK_REQ_N/GPIO_88	AC7	PX_3	DI	PCIe0 clock request	PCIe0 control signal
PCIe0_RESET_N/GPIO_87	AA7	PX_3	DO	PCIe0 reset signal	
PCIe0_WAKE_N/GPIO_89	AB7	PX_3	DI	PCIe0 wake-up signal	
PCIe1_REFCLK_P	AF7	–	AI, AO	PCIe 1 Gen 3 reference clock – positive	PCIe1 2-lane
PCIe1_REFCLK_M	AG7	–	AI, AO	PCIe 1 Gen 3 reference clock – negative	
PCIe1_TX0_P	AE6	–	AO	PCIe 1 Gen 3 Transmit lane 0 – positive	
PCIe1_TX0_M	AF6	–	AO	PCIe 1 Gen 3 Transmit lane 0 – negative	
PCIe1_RX0_P	AE8	–	AI	PCIe 1 Gen 3 receive lane 0 – positive	
PCIe1_RX0_M	AD8	–	AI	PCIe 1 Gen 3 receive lane 0 – negative	
PCIe1_TX1_P	AE7	–	AO	PCIe 1 Gen 3 Transmit lane 1 – posiive	
PCIe1_TX1_M	AD7	–	AO	PCIe 1 Gen 3 Transmit lane 1 – negative	
PCIe1_RX1_P	AF8	–	AI	PCIe 1 Gen 3 receive lane 1 – positive	
PCIe1_RX1_M	AG8	–	AI	PCIe 1 Gen 3 receive lane 1 – negative	
PCIe1_CLK_REQ_N/GPIO_79	AA9	PX_3	DI	PCIe Clock request	PCIe1 control signal
PCIe1_RESET_N/GPIO_2	AG13	PX_3	DO	PCIe reset signal	
PCIe1_WAKE_N/GPIO_3	W1	PX_3	DI	PCIe wake-up signal	

2.2.8. SDIO interface

The SOM supports 2 x 4-lane SDIO, SDC1 is non-por feature, while SDC2 is connected to SD card.

The SDIO is a high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 MHz.
- The signals routing should be 50Ω ±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

Table 2-9. SDIO interface definition

Pin name	Pin	Volt.	Type	Description	Notes
SDC1_CLK	V31	PX_7	DO	Secure digital controller 1 clock	SDC1 (no-PoR)
SDC1_CMD	W32	PX_7	B	Secure digital controller 1 command	
SDC1_DATA_0	W31	PX_7	B	Secure digital controller 1 data bit 0	
SDC1_DATA_1	U31	PX_7	B	Secure digital controller 1 data bit 1	
SDC1_DATA_2	U32	PX_7	B	Secure digital controller 1 data bit 2	
SDC1_DATA_3	V32	PX_7	B	Secure digital controller 1 data bit 3	
SDC2_CLK	P5	PX_2	DO	Secure digital controller 2 clock	SDC2
SDC2_CMD	P6	PX_2	BH	Secure digital controller 2 command	
SDC2_DATA_0	P4	PX_2	BH	Secure digital controller 2 data bit 0	
SDC2_DATA_1	P3	PX_2	BH	Secure digital controller 2 data bit 1	
SDC2_DATA_2	R6	PX_2	BH	Secure digital controller 2 data bit 2	
SDC2_DATA_3	R5	PX_2	BH	Secure digital controller 2 data bit 3	
SD_CARD_DET_N/GPIO_91	A28	PX_3	DI	SD CARD detect signal	For SD card
VREG_L6C_2P96	B21	2.96V	PO	1.65V~3.54V, 2.96V typ SD Card signal pull up power	
VREG_L9C_2P96	A22	2.96V	PO	2.7V~3.54V, 2.96V typ SD Card Power Supply	

2.2.9. SSC interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C, SPI and UART interfaces.

Table 2-10. SSC interface definition

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_159	AG17	PX_3	B B	LPI_QUP0 SE0, lane 0: I2C_SDA LPI_QUP0 SE0, lane 0: I3C_SDA	SE0
GPIO_160	AC16	PX_3	DO DO	LPI_QUP0 SE0, lane 1: I2C_SCL LPI_QUP0 SE0, lane 1: I3C_SCL	
GPIO_161	AA15	PX_3	B B	LPI_QUP0 SE1, lane 0: I2C_SDA LPI_QUP0 SE1, lane 0: I3C_SDA	SE1
GPIO_162	AF16	PX_3	DO DO	LPI_QUP0 SE1, lane 1: I2C_SCL LPI_QUP0 SE1, lane 1: I3C_SCL	
GPIO_163	AE16	PX_3	DI B DI	LPI_QUP0 SE2, lane 0: UART_CTS LPI_QUP0 SE2, lane 0: I2C_SDA LPI_QUP0 SE2, lane 0: SPI_MISO	SE2
GPIO_164	AD16	PX_3	DO DO DO	LPI_QUP0 SE2, lane 1: UART_RFR LPI_QUP0 SE2, lane 1: I2C_SCL LPI_QUP0 SE2, lane 1: SPI_MOSI	
GPIO_165	AG16	PX_3	DO DO	LPI_QUP0 SE2, lane 2: UART_TX LPI_QUP0 SE2, lane 2: SPI_SCLK	
GPIO_166	AB15	PX_3	DI DO	LPI_QUP0 SE2, lane 3: UART_RX LPI_QUP0 SE2, lane 3: SPI_CS_0	
GPIO_171	AA14	PX_3	B DO	LPI_QUP0 SE5, lane 0: I2C_SDA LPI_QUP0 SE5, lane 2: UART_TX	SE5
GPIO_172	AC15	PX_3	DO DI	LPI_QUP0 SE5, lane 1: I2C_SCL LPI_QUP0 SE5, lane 3: UART_RX	
GPIO_173	AB14	PX_3	DO	LPI_QUP0 SE6, lane 2: UART_TX	SE6
GPIO_174	AC14	PX_3	DO	LPI_QUP0 SE6, lane 3: UART_RX	

2.2.10. QUP interface

These GPIOs are available as QUP (Qualcomm universal peripheral) interface ports that can be configured for UART, SPI, I2C or I3C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus needs to be supplemented by a 2.2 kΩ pull-up resistor.

Table 2-11. QUP interface definition

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_0	H30	PX_3	DI B DI B	QUP 0 SE0, lane 0: UART_CTS QUP 0 SE0, lane 0: I2C_SDA QUP 0 SE0, lane 0: SPI_MISO QUP 0 SE0, lane 0: I3C_SDA	
GPIO_1	J28	PX_3	DO DO DO DO	QUP 0 SE0, lane 1: UART_RFR QUP 0 SE0, lane 1: I2C_SCL QUP 0 SE0, lane 1: SPI_MOSI QUP 0 SE0, lane 1: I3C_SCL	
PCIe1_RESET_N/GPIO_2	AG13	PX_3	DO DO DO	QUP 0 SE0, lane 2: UART_TX QUP 0 SE0, lane 2: SPI_SCLK QUP 0 SE7, lane 4: SPI_CS_1	Default for PCIe use
PCIe1_WAKE_N/GPIO_3	W1	PX_3	DO DO DO	QUP0 SE0, lane 3: UART_RX QUP0 SE0, lane 3: SPI_CS_0 QUP0 SE7, lane 5: SPI_CS_2	Default for PCIe use
GPIO_4	J24	PX_3	DI B DI B	QUP0 SE1, lane 0 UART_CTS QUP0 SE1, lane 0 I2C_SDA QUP0 SE1, lane 0 SPI_MISO QUP 0 SE1, lane 0: I3C_SDA	
GPIO_5	H22	PX_3	DO DO DO DO	QUP0 SE1, lane 1:UART_RFR QUP0 SE1, lane 1: I2C_SCL QUP0 SE1, lane 1: SPI_MOSI QUP 0 SE1, lane 1: I3C_SCL	
GPIO_6	AE12	PX_3	DO DO DO	QUP0 SE1, lane 2: UART_TX QUP0 SE1, lane 2: SPI_SCLK QUP0 SE7, lane 6: SPI_CS_3	
GPIO_7	J31	PX_3	DI DO	QUP0 SE1, lane 3: UART_RX QUP0 SE1, lane 3: SPI_CS_0	
GPIO_8	J30	PX_3	DI B DI	QUP0 SE2, lane 0: UART_CTS QUP0 SE2, lane 0: I2C_SDA QUP0 SE2, lane 0: SPI_MISO	
GPIO_9	J27	PX_3	DO DO DO	QUP0 SE2, lane 1: UART_RFR QUP0 SE2, lane 1: I2C_SCL QUP0 SE2, lane 1: SPI_MOSI	
GPIO_10	AD2	PX_3	DO DO	QUP0 SE2, lane 2: UART_TX QUP0 SE2, lane 2: SPI_SCLK	
GPIO_11	J29	PX_3	DI DO	QUP0 SE2, lane 3: UART_RX QUP0 SE2, lane 3: SPI_CS_0	

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_12	AF12	PX_3	DI B DI	QUP0 SE3, lane 0: UART_CTS QUP0 SE3, lane 0: I2C_SDA QUP0 SE3, lane 0: SPI_MISO	
GPIO_13	AG5	PX_3	DO DO DO	QUP0 SE3, lane 1: UART_RFR QUP0 SE3, lane 1: I2C_SCL QUP0 SE3, lane 1: SPI_MOSI	
GPIO_14	AC8	PX_3	DO DO DI	QUP0 SE3, lane 2: UART_TX QUP0 SE3, lane 2: SPI_SCLK Boot configuration control bit 12	
GPIO_15	AE5	PX_3	DI DO DI	QUP0 SE3, lane 3: UART_RX QUP0 SE3, lane 3: SPI_CS_0 Boot configuration control bit 9	
GPIO_16	AC5	PX_3	DI B DI	QUP0 SE4, lane 0: UART_CTS QUP0 SE4, lane 0: I2C_SDA QUP0 SE4, lane 0: SPI_MISO	
GPIO_17	AD5	PX_3	DO DO DO	QUP0 SE4, lane 1: UART_RFR QUP0 SE4, lane 1: I2C_SCL QUP0 SE4, lane 1: SPI_MOSI	
GPIO_18	AB8	PX_3	DO DO	QUP0 SE4, lane 2: UART_TX QUP0 SE4, lane 2: SPI_SCLK	
GPIO_19	AB5	PX_3	DI DO	QUP0 SE4, lane 3: UART_RX QUP0 SE4, lane 3: SPI_CS_0	
GPIO_20	U27	PX_3	DI B DI	QUP0 SE5, lane 0: UART_CTS QUP0 SE5, lane 0: I2C_SDA QUP0 SE5, lane 0: SPI_MISO	
GPIO_21	T28	PX_3	DO DO DO	QUP0 SE5, lane 1: UART_RFR QUP0 SE5, lane 1: I2C_SCL QUP 0 SE5, lane 1: SPI_MOSI	
DBG_UART_TX/GPIO_22	U28	PX_3	DO DO	QUP0 SE5, lane 2: UART_TX (UART debug port) QUP0 SE5, lane 2: SPI_SCLK	Default for UART debug
DBG_UART_RX/GPIO_23	V28	PX_3	DI DO	QUP0 SE5, lane 3: UART_RX (UART debug port) QUP0 SE5, lane 3: SPI_CS_0	Default for UART debug
GPIO_24	AC6	PX_3	DI B DI	QUP0 SE6, lane 0: UART_CTS QUP0 SE6, lane 0: I2C_SDA QUP0 SE6, lane 0: SPI_MISO	
GPIO_25	AD6	PX_3	DO DO DO	QUP0 SE6, lane 1: UART_RFR QUP0 SE6, lane 1: I2C_SCL QUP0 SE6, lane 1: SPI_MOSI	
GPIO_26	AA6	PX_3	DO DO	QUP0 SE6, lane 2: UART_TX QUP0 SE6, lane 2: SPI_SCLK	

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_27	AB6	PX_3	DI DO	QUP0 SE6, lane 3: UART_RX QUP0 SE6, lane 3: SPI_CS_0	
GPIO_28	AA5	PX_3	DI B DI	QUP0 SE7, lane 0: UART_CTS QUP0 SE7, lane 0: I2C_SDA QUP0 SE7, lane 0: SPI_MISO	
GPIO_29	Y5	PX_3	DO DO DO	QUP0 SE7, lane 1: UART_RFR QUP0 SE7, lane 1: I2C_SCL QUP0 SE7, lane 1: SPI_MOSI	
GPIO_30	AB4	PX_3	DO DO	QUP0 SE7, lane 2: UART_TX QUP0 SE7, lane 2: SPI_SCLK	
GPIO_31	AA4	PX_3	DI DO	QUP0 SE7, lane 3: UART_RX QUP0 SE7, lane 3: SPI_CS_0	
GPIO_32	R26	PX_3	DI B DI	QUP1 SE0, lane 0: UART_CTS QUP1 SE0, lane 0: I2C_SDA QUP1 SE0, lane 0: SPI_MISO	
GPIO_33	T26	PX_3	DO DO DO	QUP1 SE0, lane 1: UART_RFR QUP1 SE0, lane 1: I2C_SCL QUP1 SE0, lane 1: SPI_MOSI	
GPIO_34	R25	PX_3	DO DO	QUP1 SE0, lane 2: UART_TX QUP1 SE0, lane 2: SPI_SCLK	
GPIO_35	T25	PX_3	DI DO	QUP1 SE0, lane 3: UART_RX QUP1 SE0, lane 3: SPI_CS_0	
GPIO_36	T23	PX_3	DI B DI B	QUP1 SE1, lane 0: UART_CTS QUP1 SE1, lane 0: I2C_SDA QUP1 SE1, lane 0: SPI_MISO QUP 1SE1, lane 0: I3C_SDA	
GPIO_37	R23	PX_3	DO DO DO DO	QUP1 SE1, lane 1: UART_RFR QUP1 SE1, lane 1: I2C_SCL QUP1 SE1, lane 1: SPI_MOSI QUP 1SE1, lane 1: I3C_SCL	
GPIO_38	T24	PX_3	DO DO DO	QUP1 SE1, lane 2: UART_TX QUP1 SE1, lane 2: SPI_SCLK QUP1 SE4, lane 6: SPI_CS_3	
GPIO_39	R24	PX_3	DI DO	QUP1 SE1, lane 3: UART_RX QUP1 SE1, lane 3: SPI_CS_0	
GPIO_40	AA3	PX_3	DI B DI	QUP1 SE2, lane 0: UART_CTS QUP1 SE2, lane 0: I2C_SDA QUP1 SE2, lane 0: SPI_MISO	
GPIO_41	AB2	PX_3	DO DO DO	QUP1 SE2, lane 1: UART_RFR QUP1 SE2, lane 1: I2C_SCL QUP1 SE2, lane 1: SPI_MOSI	
GPIO_42	AB3	PX_3	DO DO	QUP1 SE2, lane 2: UART_TX QUP1 SE2, lane 2: SPI_SCLK	

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_43	AC2	PX_3	DI DO	QUP1 SE2, lane 3: UART_RX QUP1 SE2, lane 3: SPI_CS_0	
GPIO_44	AF13	PX_3	DI B DI	QUP1 SE3, lane 0: UART_CTS QUP1 SE3, lane 0: I2C_SDA QUP1 SE3, lane 0: SPI_MISO	
GPIO_45	M22	PX_3	DO DO DO	QUP1 SE3, lane 1: UART_RFR QUP1 SE3, lane 1: I2C_SCL QUP1 SE3, lane 1: SPI_MOSI	
GPIO_46	M5	PX_3	DO DO	QUP1 SE3, lane 2: UART_TX QUP1 SE3, lane 2: SPI_SCLK	
GPIO_47	M6	PX_3	DI DO DI	QUP1 SE3, lane 3: UART_RX QUP1 SE3, lane 3: SPI_CS_0 DisplayPort hot plug detect	
GPIO_48	U23	PX_3	DI B DI	QUP1 SE4, lane 0: UART_CTS QUP1 SE4, lane 0: I2C_SDA QUP1 SE4, lane 0: SPI_MISO	
GPIO_49	T22	PX_3	DO DO DO	QUP1 SE4, lane 1: UART_RFR QUP1 SE4, lane 1: I2C_SCL QUP1 SE4, lane 1: SPI_MOSI	
GPIO_50	U24	PX_3	DO DO DO	QUP1 SE4, lane 2: UART_TX QUP1 SE4, lane 2: SPI_SCLK QUP1 SE6, lane 6: SPI_CS_3	
GPIO_51	U22	PX_3	DI DO	QUP1 SE4, lane 3: UART_RX QUP1 SE4, lane 3: SPI_CS_0	
GPIO_52	V25	PX_3	DI B DI	QUP1 SE5, lane 0: UART_CTS QUP1 SE5, lane 0: I2C_SDA QUP1 SE5, lane 0: SPI_MISO	
GPIO_53	U26	PX_3	DO DO DO	QUP1 SE5, lane 1: UART_RFR QUP1 SE5, lane 1: I2C_SCL QUP1 SE5, lane 1: SPI_MOSI	
GPIO_54	R27	PX_3	DO DO DO	QUP1 SE5, lane 2: UART_TX QUP1 SE5, lane 2: SPI_SCLK QUP1 SE4, lane 5: SPI_CS_2	
GPIO_55	V26	PX_3	DI DO DO	QUP1 SE5, lane 3: UART_RX QUP1 SE5, lane 3: SPI_CS_0 QUP1 SE4, lane 4: SPI_CS_1	
GPIO_56	U25	PX_3	DI B DI	QUP1 SE6, lane 0: UART_CTS QUP1 SE6, lane 0: I2C_SDA QUP1 SE6, lane 0: SPI_MISO	
GPIO_57	V23	PX_3	DO DO DO	QUP1 SE6, lane 1: UART_RFR QUP1 SE6, lane 1: I2C_SCL QUP1 SE6, lane 1: SPI_MOSI	

Pin name	Pin	Voltage	Type	Description	Notes
GPIO_58	V22	PX_3	DO DO	QUP1 SE6, lane 2: UART_TX QUP1 SE6, lane 2: SPI_SCLK	
GPIO_59	V24	PX_3	DI DO	QUP1 SE6, lane 3: UART_RX QUP1 SE6, lane 3: SPI_CS_0	
GPIO_60	AA8	PX_3	DI B DI DI	QUP1 SE7, lane 0: UART_CTS QUP1 SE7, lane 0: I2C_SDA QUP1 SE7, lane 0: SPI_MISO eDP hot plug detect	
GPIO_61	AC4	PX_3	DO DO DO DO	QUP1 SE7, lane 1: UART_RFR QUP1 SE7, lane 1: I2C_SCL QUP1 SE7, lane 1: SPI_MOSI Secure digital card write protection	
GPIO_62	AC3	PX_3	DO DO DO	QUP1 SE7, lane 2: UART_TX QUP1 SE7, lane 2: SPI_SCLK QUP1 SE6, lane 4: SPI_CS_1	
GPIO_63	AD3	PX_3	DI DO DO DI	QUP1 SE7, lane 3: UART_RX QUP1 SE7, lane 3: SPI_CS_0 QUP1 SE6, lane 5: SPI_CS_2 Boot configuration control bit 11	

2.2.11. Debug UART interface

Table 2-12. Debug UART interface definition

Pin name	Pin	Voltage	Type	Description	Notes
DBG_UART_TX/GPIO_22	U28	PX_3	DO	QUP0 SE5, lane 2: UART_TX	Default for UART debug
DBG_UART_RX/GPIO_23	V28	PX_3	DI	QUP0 SE5, lane 3: UART_RX	

2.2.12. Power on interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the available power sources of the device, and enable the correct source. Press the KPD_PWR_N for ~2 s to boot the system properly. Power on/off key signal can be connected to ground through SOM Pin M8, PHONE_ON_N (200 kΩ internally pulled up to 1.1 V).

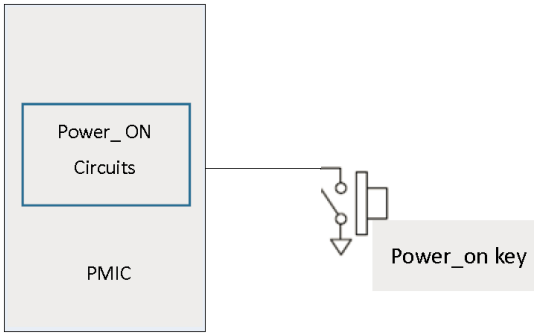

Figure 2-1.Power on Signal

Table 2-13. Power on interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PHONE_ON_N	AD29	–	DI	Power-on key ground switch (200 kΩ internal PU to 1.1 V)	

2.2.13. Reset interface

You can generate a mandatory reset by a long key press of RESIN_N, KPD_PWR_N, or RESIN_N plus KPD_PWR_N in combination.

Table 2-14. Reset interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PM_RESIN_N	E6	40kΩ internal PU to 1.8 V	DI	Volume down/Reset key signal, Low active	

2.2.14. Keys interface

Table 2-15. Keys interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PHONE_ON_N	AD29	200kΩ internal PU to 1.1 V	DI	Power-on key ground switch	
KYPD_VOL_UP_N	B29	–	DI	Keypad volume up button	
PM_RESIN_N	E6	40kΩ internal PU to 1.8 V	DI	Reset; Keypad volume down button	

2.2.15. Battery interface

Battery interfaces are special for battery interface, major for monitoring battery status, inserting and voltage detection.

Table 2-16. Battery interface definition

Pin name	Pin	Voltage	Type	Description	Notes
BATT_THERM	AF25	1.875V max	AI	Battery temperature input to ADC for measuring the pack temperature. Used for charger safe operation and BMS. 100K pull down, or connect to Battery	
BATT_ID	AE29	1.875V max	AI	Battery ID input to the ADC interface. Used for missing battery detection. 100K pull down, or connect to Battery	
VBATT_VSNS_P	AC24	–	AI	Battery voltage sense input plus. Connect to the battery positive remote sense node or connect this directly to the battery positive node.	
VBATT_VSNS_M	AD24	–	AI	Battery voltage sense input minus. Connect to the battery negative remote sense node or connect this directly to the battery negative node.	
VBATT_PACK_SNS_M	AC25	–	AI	Battery voltage sense input minus. Directly to the battery negative node (pack negative).	
VBATT_OPT_ISNS_P	AG26	–	AI	Battey current sense positive node (reserved).	
VBATT_OPT_ISNS_M	AG27	–	AI	Battey current sense negative node (reserved).	

2.2.16. PMIC GPIOs

The PMICs provide GPIO with different functions.

Table 2-17. PMICs and GPIOs

PMIC	Pin name	Pin	Voltage	Description	Notes
PMK7325	PMK_GPIO_01	AA16	LV	Configurable; default digital input with 10 µA pull-down	AMUX SMB_SPMI_CLK
	PMK_GPIO_02	AB16	LV	Configurable; default digital input with 10 µA pull-down	AMUX SMB_SPMI_DATA
PM7250B	PM_A_GPIO_01	AF27	LV	Configurable; default digital input with 10 µA pull-down	AMUX
	PM_A_GPIO_02	E2	LV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_03	E1	LV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_04	E3	LV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_05	AG29	MV	Configurable; default digital input with 10 µA pull-down	AMUX
	PM_A_GPIO_06	D1	MV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_07	AB30	MV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_08	AG28	MV	Configurable; default digital input with 10 µA pull-down	AMUX
	PM_A_GPIO_09	AF29	LV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_10	AE28	LV	Configurable; default digital input with 10 µA pull-down	-
	PM_A_GPIO_11	AE26	LV	Configurable; default digital input with 10 µA pull-down	AMUX
	PM_A_GPIO_12	AB25	LV	Configurable; default digital input with 10 µA pull-down	AMUX
PM7325	PM_B_GPIO_01	K29	LV	Configurable; default digital input with 10 µA pull-down	PM7325 GPIO_01
	PM_B_GPIO_04	C28	LV	Configurable; default digital input with 10 µA pull-down	PM7325 GPIO_04
	PM_B_GPIO_05	A29	MV	Configurable; default digital input with 10 µA pull-down	PM7325_GPIO_05 CBL_PWR_N
	PM_B_GPIO_08	E5	MV	Configurable; default digital input with 10 µA pull-down	PM7325 GPIO_08
	PM_B_GPIO_09	E4	MV	Configurable; default digital input with 10 µA pull-down	PM7325 GPIO_09
	PM_B_AMUX2	C27	AI	Analog multiplexer (AMUX) input 2	PM7325 AMUX_2
	PM_B_AMUX4	B28	AI	Analog multiplexer (AMUX) input 4	PM7325 AMUX_4

PMIC	Pin name	Pin	Voltage	Description	Notes
PM7350C	PM_C_GPIO_01	F25	LV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_01
	PM_C_GPIO_02	F26	LV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_02
	PM_C_GPIO_03	F24	LV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_03
	PM_C_GPIO_04	D24	LV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_04
	PM_C_GPIO_05	D2	MV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_05
	PM_C_GPIO_06	D28	MV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_06
	PM_C_GPIO_07	C24	MV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_07
	PM_C_GPIO_08	B24	MV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_08
	PM_C_GPIO_09	C29	MV	Configurable; default digital input with 10 µA pull-down	PM7350C GPIO_09

2.2.17. PWMs and LED current driver interface

The SOM has two PWM outputs and three LED current drivers.

Table 2-18. PWMs and LED current driver interface definition

Pin name	Pin	Voltage	Type	Description	Notes
PWM signals					
PM_C_GPIO_08	B24	MV	DO	Can be configured as GPIO and PWM (Only GPIO_08 is available for fixed duty cycle variable frequency mode.)	
PM_C_GPIO_09	C29	MV	DO		
LED signals					
IRIS_RED	D29	–	AO	Independent high-side current source brightness control of red, green, and blue channels, 12 mA maximum per channel	
IRIS_GREEN	E28	–	AO		
IRIS_BLUE	C26	–	AO		

2.2.18. JTAG interface

The SOM provides JTAG for software debug.

Table 2-19. JTAG interface definition

Name	Pin	Voltage	Type	Description	Notes
JTAG_SRST_N	H23	PX_3	DI	JTAG reset for debug	
JTAG_TCK	H25	PX_3	DI	JTAG clock input	
JTAG_TDI	J26	PX_3	DI	JTAG data input	
JTAG_TDO	H26	PX_3	DO-Z	JTAG data output	
JTAG_TMS	J25	PX_3	DI	JTAG mode select input	
JTAG_TRST_N	H24	PX_3	DI	JTAG reset	

2.3. Pin summary

Table 2-20. Pin summary

Pin	Pin Name	Voltage	Pin Type	Notes
AF20	VBATT1	–	PI, PO	
AF21	VBATT2			
AF22	VBATT3			
AF23	VBATT4			
AG20	VBATT5			
AG21	VBATT6			
AG22	VBATT7			
AG23	VBATT8			
AG27	VBATT_OPT_ISNS_M	–	AI	Battery interface
AG26	VBATT_OPT_ISNS_P	–	AI	
AD24	VBATT_VSNS_M	–	AI	
AC24	VBATT_VSNS_P	–	AI	
AC25	VBATT_PACK_SNS_M	–	AI	
AF25	BATT_THERM	1.875V max	AI	
AE29	BATT_ID	1.875V max	AI	
AB31	VPH_PWR1	–	PO	
AB32	VPH_PWR2			
AC30	VPH_PWR3			
AC31	VPH_PWR4			
AC32	VPH_PWR5			
AD30	VPH_PWR6			
AD31	VPH_PWR7			
AD32	VPH_PWR8			
Y22	USB_VBUS1	–	PI, PO	Input power from the USB source, or output during USB-OTG.
Y23	USB_VBUS2			
AA22	USB_VBUS3			
AA23	USB_VBUS4			
AB22	USB_VBUS5			
AB23	USB_VBUS6			
AC22	USB_VBUS7			
AC23	USB_VBUS8			
B20	VCOIN	2V~3.25V	PI, PO	Coin-cell charge and supply
E25	PMIC_SPMI_CLK	PX_0	DO	Slave and PBUS interface for PMICs – clock
E26	PMIC_SPMI_DATA	PX_0	BH	Slave and PBUS interface for PMICs – data
AA16	PMK_GPIO_01	LV	DI, DO	

Pin	Pin Name	Voltage	Pin Type	Notes
AB16	PMK_GPIO_02	LV	DI, DO	
AE25	SMB_THERM	1.875V max	AI	SQC6490 SOM reserved pin. Please keep it floating.
AD27	SMB_EN	LV	DO	SQC6490 SOM reserved pin. Please keep it floating.
Y24	PMB_MID_CHG1	-	-	SQC6490 SOM reserved pin. Please keep it floating.
Y25	PMB_MID_CHG2			
Y26	PMB_MID_CHG3			
Y27	PMB_MID_CHG4			
AA24	PMB_MID_CHG5			
AA25	PMB_MID_CHG6			
AA26	PMB_MID_CHG7			
AA27	PMB_MID_CHG8			
C20	VREG_BOB1	3.3V	PO	Will increase to 3.6V during the bootup of the SOM
C21	VREG_BOB2			
D20	VREG_BOB3			
D21	VREG_BOB4			
AG30	VREG_L16B_1P2	1.2V	PO	
AE20	VREG_L17B_1P8	1.8V	PO	
E24	VREG_L18B_1P8	1.8V	PO	
D22	VREG_L2B_3P072	3.072V	PO	
A21	VREG_L3C_3P0	3V	PO	
A23	VREG_L4C_1P8_3P0	1.8V	PO	
F23	VREG_L2C_1P8	1.8V	PO	
W4	VREG_L7C_3P0	3V	PO	
D23	VREG_L8C_1P8	1.8V	PO	
B23	VREG_L11C_2P8	2.8V	PO	
E22	VREG_L12C_1P8	1.8V	PO	
A24	VREG_L13C_3P0	3.0V	PO	
W26	VREG_SYS_1P8	1.8V	PO	
AC29	VIB_DRV_P	-	PO	
J5	CSI0_NC_CLK_P	CSI	AI	D-PHY
J4	CSI0_A0_CLK_M			
J2	CSI0_B0_LN0_P			
J1	CSI0_C0_LN0_M			
K5	CSI0_A1_LN1_P			
K6	CSI0_B1_LN1_M			
K4	CSI0_C1_LN2_P			
K3	CSI0_A2_LN2_M			
K2	CSI0_B2_LN3_P			
K1	CSI0_C2_LN3_M			

Pin	Pin Name	Voltage	Pin Type	Notes
B5	CSI1_NC_CLK_P	CSI	AI	D-PHY C-PHY
A5	CSI1_A0_CLK_M			
C6	CSI1_B0_LN0_P			
B6	CSI1_C0_LN0_M			
C5	CSI1_A1_LN1_P			
D5	CSI1_B1_LN1_M			
A4	CSI1_C1_LN2_P			
B4	CSI1_A2_LN2_M			
D4	CSI1_B2_LN3_P			
C4	CSI1_C2_LN3_M			
F1	CSI2_NC_CLK_P	CSI	AI	D-PHY
F2	CSI2_A0_CLK_M			
G1	CSI2_B0_LN0_P			
G2	CSI2_C0_LN0_M			
F5	CSI2_A1_LN1_P			
F4	CSI2_B1_LN1_M			
G6	CSI2_C1_LN2_P			
G5	CSI2_A2_LN2_M			
G4	CSI2_B2_LN3_P			
G3	CSI2_C2_LN3_M			
B9	CSI3_NC_CLK_P	CSI	AI	D-PHY C-PHY
C9	CSI3_A0_CLK_M			
A8	CSI3_B0_LN0_P			
B8	CSI3_C0_LN0_M			
C8	CSI3_A1_LN1_P			
D8	CSI3_B1_LN1_M			
C7	CSI3_C1_LN2_P			
D7	CSI3_A2_LN2_M			
A7	CSI3_B2_LN3_P			
B7	CSI3_C2_LN3_M			
C12	CSI4_NC_CLK_P	CSI	AI	D-PHY
B12	CSI4_A0_CLK_M			
A11	CSI4_B0_LN0_P			
B11	CSI4_C0_LN0_M			
C11	CSI4_A1_LN1_P			
D11	CSI4_B1_LN1_M			
C10	CSI4_C1_LN2_P			
D10	CSI4_A2_LN2_M			
A10	CSI4_B2_LN3_P			
B10	CSI4_C2_LN3_M			
U5	CAM_MCLK0/GPIO_64	PX_3	DO	

Pin	Pin Name	Voltage	Pin Type	Notes
R4	CAM_MCLK1/GPIO_65	PX_3	DO	
T4	CAM_MCLK2/GPIO_66	PX_3	DO	
T5	CAM_MCLK3/GPIO_67	PX_3	DO	
R3	CAM_MCLK4/GPIO_68	PX_3	DO	
U4	CAM_MCLK5/GPIO_93	PX_3	DO	
AA1	CCI_I2C0_SDA/GPIO_69	PX_3	B	
Y1	CCI_I2C0_SCL/GPIO_70	PX_3	DO	
AC1	CCI_I2C1_SDA/GPIO_71	PX_3	B	
AB1	CCI_I2C1_SCL/GPIO_72	PX_3	DO	
AA2	CCI_I2C2_SDA/GPIO_73	PX_3	B	
Y2	CCI_I2C2_SCL/GPIO_74	PX_3	DO	
W6	CCI_I2C3_SDA/GPIO_75	PX_3	B	
Y6	CCI_I2C3_SCL/GPIO_76	PX_3	DO	
C16	DSI0_B1_CLK_P	DSI	AO	D-PHY
D16	DSI0_C1_CLK_M			
B16	DSI0_A0_LN0_P			
A16	DSI0_B0_LN0_M			
B17	DSI0_C0_LN1_P			
A17	DSI0_A1_LN1_M			
A18	DSI0_A2_LN2_P			
B18	DSI0_B2_LN2_M			
C17	DSI0_C2_LN3_P			
D17	DSI0_NC_LN3_M			
AD10	PCIe0_REFCLK_M	–	AI, AO	PCIe0
AE10	PCIe0_REFCLK_P	–	AI, AO	
AE11	PCIe0_RX_M	–	AI	
AD11	PCIe0_RX_P	–	AI	
AE9	PCIe0_TX_M	–	AO	
AF9	PCIe0_TX_P	–	AO	
AC7	PCIe0_CLK_REQ_N/GPIO_88	PX_3	DI	PCIe0 clock request
AA7	PCIe0_RESET_N/GPIO_87	PX_3	DO	PCIe0 reset signal
AB7	PCIe0_WAKE_N/GPIO_89	PX_3	DI	PCIe0 wake-up signal
AG7	PCIe1_REFCLK_M	–	AI, AO	PCIe1
AF7	PCIe1_REFCLK_P	–	AI, AO	
AD8	PCIe1_RX0_M	–	AI	
AE8	PCIe1_RX0_P	–	AI	
AG8	PCIe1_RX1_M	–	AI	
AF8	PCIe1_RX1_P	–	AI	
AF6	PCIe1_TX0_M	–	AO	
AE6	PCIe1_TX0_P	–	AO	

Pin	Pin Name	Voltage	Pin Type	Notes
AD7	PCIe1_TX1_M	–	AO	
AE7	PCIe1_TX1_P	–	AO	
AA9	PCIe1_CLK_REQ_N/GPIO_79	PX_3	DI	PCIe1 clock request
AG13	PCIe1_RESET_N/GPIO_2	PX_3	DO	PCIe1 reset signal
W1	PCIe1_WAKE_N/GPIO_3	PX_3	DI	PCIe1 wake-up signal
V31	SDC1_CLK	PX_7	DO	SDC1 (no-PoR)
W32	SDC1_CMD	PX_7	B	
W31	SDC1_DATA_0	PX_7	B	
U31	SDC1_DATA_1	PX_7	B	
U32	SDC1_DATA_2	PX_7	B	
V32	SDC1_DATA_3	PX_7	B	
P5	SDC2_CLK	PX_2	DO	SDC2
P6	SDC2_CMD	PX_2	BH	
P4	SDC2_DATA_0	PX_2	BH	
P3	SDC2_DATA_1	PX_2	BH	
R6	SDC2_DATA_2	PX_2	BH	
R5	SDC2_DATA_3	PX_2	BH	
A28	SD_CARD_DET_N/GPIO_91	PX_3	DI	SD CARD detect signal
B21	VREG_L6C_2P96	1.8V /2.96V	PO	SD Card signal pull up power
A22	VREG_L9C_2P96	2.96V	PO	SD Card Power Supply
R32	USB0_HS_DM	–	AI, AO	USB0 Type-C (with DP)
R31	USB0_HS_DP	–	AI, AO	
N32	USB0_SS_RX0_M	–	AI	
N31	USB0_SS_RX0_P	–	AI	
P32	USB0_SS_RX1_M	–	AI	
P31	USB0_SS_RX1_P	–	AI	
M31	USB0_SS_TX0_M	–	AO	
M32	USB0_SS_TX0_P	–	AO	
L31	USB0_SS_TX1_M	–	AO	
L32	USB0_SS_TX1_P	–	AO	
K31	USB0_DP_AUX_M	–	AI, AO	
K32	USB0_DP_AUX_P	–	AI, AO	
AG25	USB0_CC1	–	AI, AO	
AG24	USB0_CC2	–	AI, AO	
AE24	USB0_SBU1	–	DI	
AF24	USB0_SBU2	–	DO	
AD25	USB_SS-H_HS-L_SEL	PX_3	DI	SQC6490 SOM reserved pin. Please keep it floating.
AE27	USB0_THERM	1.875V max	AI	USB connector temperature detection

Pin	Pin Name	Voltage	Pin Type	Notes
AF30	PM_USB_OPTION	1.875V max	AI	SQC6490 SOM reserved pin. Please keep it floating.
V3	USB1_HS_DP	–	AI, AO	USB1
V4	USB1_HS_DM	–	AI, AO	
AF28	FORCED_USB_BOOT/GPIO_82	PX_3	DI	Forces a USB boot, active high
B29	KYPD_VOL_UP_N	–	DI	
E6	PM_RESIN_N	–	DI	
AD29	PHONE_ON_N	–	DI	
AD28	FAULT_N	1.8V	DO, DI	Test pin. Keep it floating.
U28	DBG_UART_TX/GPIO_22	PX_3	DO	
V28	DBG_UART_RX/GPIO_23	PX_3	DI	
AC28	SLEEP_CLK	1.8V	AO	32.7645 kHz sleep clock output (1.8 V)
L23	BOOT_CONFIG_0/GPIO_118	PX_3	DI	Boot configuration control bit 0
L24	BOOT_CONFIG_1/GPIO_120	PX_3	DI	Boot configuration control bit 1
L22	BOOT_CONFIG_2/GPIO_122	PX_3	DI	Boot configuration control bit 2
N24	BOOT_CONFIG_3/GPIO_124	PX_3	DI	Boot configuration control bit 3
M23	BOOT_CONFIG_4/GPIO_126	PX_3	DI	Boot configuration control bit 4
M24	BOOT_CONFIG_5	PX_3	DI	SQC6490 SOM reserved pin. Please keep it floating.
H23	JTAG_SRST_N	PX_3	DI	JTAG reset for debug
H25	JTAG_TCK	PX_3	DI	JTAG clock input
J26	JTAG_TDI	PX_3	DI	JTAG data input
H26	JTAG_TDO	PX_3	DO-Z	JTAG data output
J25	JTAG_TMS	PX_3	DI	JTAG mode select input
H24	JTAG_TRST_N	PX_3	DI	JTAG reset
D29	IRIS_RED	–	AO	Red LED
E28	IRIS_GREEN	–	AO	Green LED
C26	IRIS_BLUE	–	AO	Blue LED
H30	GPIO_0	PX_3		
J28	GPIO_1	PX_3		
J24	GPIO_4	PX_3		
H22	GPIO_5	PX_3		
AE12	GPIO_6	PX_3		
J31	GPIO_7	PX_3		
J30	GPIO_8	PX_3		
J27	GPIO_9	PX_3		

Pin	Pin Name	Voltage	Pin Type	Notes
AD2	GPIO_10	PX_3		
J29	GPIO_11	PX_3		
AF12	GPIO_12	PX_3		
AG5	GPIO_13	PX_3		
AC8	GPIO_14	PX_3		
AE5	GPIO_15	PX_3		
AC5	GPIO_16	PX_3		
AD5	GPIO_17	PX_3		
AB8	GPIO_18	PX_3		
AB5	GPIO_19	PX_3		
U27	GPIO_20	PX_3		
T28	GPIO_21	PX_3		
AC6	GPIO_24	PX_3		
AD6	GPIO_25	PX_3		
AA6	GPIO_26	PX_3		
AB6	GPIO_27	PX_3		
AA5	GPIO_28	PX_3		
Y5	GPIO_29	PX_3		
AB4	GPIO_30	PX_3		
AA4	GPIO_31	PX_3		
R26	GPIO_32	PX_3		
T26	GPIO_33	PX_3		
R25	GPIO_34	PX_3		
T25	GPIO_35	PX_3		
T23	GPIO_36	PX_3		
R23	GPIO_37	PX_3		
T24	GPIO_38	PX_3		
R24	GPIO_39	PX_3		
AA3	GPIO_40	PX_3		
AB2	GPIO_41	PX_3		
AB3	GPIO_42	PX_3		
AC2	GPIO_43	PX_3		
AF13	GPIO_44	PX_3		
M22	GPIO_45	PX_3		
M5	GPIO_46	PX_3		
M6	GPIO_47	PX_3		
U23	GPIO_48	PX_3		
T22	GPIO_49	PX_3		
U24	GPIO_50	PX_3		
U22	GPIO_51	PX_3		
V25	GPIO_52	PX_3		

Pin	Pin Name	Voltage	Pin Type	Notes
U26	GPIO_53	PX_3		
R27	GPIO_54	PX_3		
V26	GPIO_55	PX_3		
U25	GPIO_56	PX_3		
V23	GPIO_57	PX_3		
V22	GPIO_58	PX_3		
V24	GPIO_59	PX_3		
AA8	GPIO_60	PX_3		
AC4	GPIO_61	PX_3		
AC3	GPIO_62	PX_3		
AD3	GPIO_63	PX_3		
V30	GPIO_77	PX_3		
T30	GPIO_78	PX_3		
U29	GPIO_80	PX_3		
L1	GPIO_81	PX_3		
AG18	GPIO_83	PX_3		
W2	GPIO_84	PX_3		
R22	GPIO_85	PX_3		
H29	GPIO_86	PX_3		
H28	GPIO_90	PX_3		
J23	GPIO_94	PX_3		
G30	GPIO_95	PX_3		
AA12	GPIO_96	PX_3		
AC11	GPIO_97	PX_3		
AB10	GPIO_98	PX_3		
AC10	GPIO_99	PX_3		
AA11	GPIO_100	PX_3		
AC12	GPIO_101	PX_3		
AB12	GPIO_102	PX_3		
AD12	GPIO_103	PX_3		
AB11	GPIO_104	PX_3		
AE14	GPIO_105	PX_3		
AB13	GPIO_106	PX_3		
AG14	GPIO_107	PX_3		
AA13	GPIO_108	PX_3		
V27	GPIO_117	PX_3		
N6	GPIO_119	PX_3		
H32	GPIO_121	PX_3		
J22	GPIO_123	PX_3		
H27	GPIO_125	PX_3		
G31	GPIO_127	PX_3		

Pin	Pin Name	Voltage	Pin Type	Notes
AE17	GPIO_128	PX_3		
U30	GPIO_129	PX_3		
T29	GPIO_130	PX_3		
AF5	GPIO_131	PX_3		
AE13	GPIO_132	PX_3		
V29	GPIO_133	PX_3		
T27	GPIO_134	PX_3		
N23	GPIO_135	PX_3		
H31	GPIO_136	PX_3		
N4	GPIO_137	PX_3		
N22	GPIO_138	PX_3		
G32	GPIO_141	PX_3		
AD1	GPIO_142	PX_3		
AE19	GPIO_144	PX_3		
AF19	GPIO_145	PX_3		
AG19	GPIO_146	PX_3		
AF18	GPIO_147	PX_3		
AD18	GPIO_148	PX_3		
AD17	GPIO_149	PX_3		
AA21	GPIO_150	PX_3		
AA20	GPIO_151	PX_3		
AA19	GPIO_152	PX_3		
AB19	GPIO_153	PX_3		
AA17	GPIO_154	PX_3		
AE18	GPIO_155	PX_3		
AA18	GPIO_156	PX_3		
AD19	GPIO_157	PX_3		
AC19	GPIO_158	PX_3		
AG17	GPIO_159	PX_3		
AC16	GPIO_160	PX_3		
AA15	GPIO_161	PX_3		
AF16	GPIO_162	PX_3		
AE16	GPIO_163	PX_3		
AD16	GPIO_164	PX_3		
AG16	GPIO_165	PX_3		
AB15	GPIO_166	PX_3		
AA14	GPIO_171	PX_3		
AC15	GPIO_172	PX_3		
AB14	GPIO_173	PX_3		
AC14	GPIO_174	PX_3		
AF27	PM_A_GPIO_01	LV	DI, DO	

Pin	Pin Name	Voltage	Pin Type	Notes
E2	PM_A_GPIO_02	LV	DI, DO	
E1	PM_A_GPIO_03	LV	DI, DO	
E3	PM_A_GPIO_04	LV	DI, DO	
AG29	PM_A_GPIO_05	MV	DI, DO	
D1	PM_A_GPIO_06	MV	DI, DO	
AB30	PM_A_GPIO_07	MV	DI, DO	
AG28	PM_A_GPIO_08	MV	DI, DO	
AF29	PM_A_GPIO_09	LV	DI, DO	
AE28	PM_A_GPIO_10	LV	DI, DO	
AE26	PM_A_GPIO_11	LV	DI, DO	
AB25	PM_A_GPIO_12	LV	DI, DO	
K29	PM_B_GPIO_01	LV	DI, DO	
C28	PM_B_GPIO_04	LV	DI, DO	
A29	PM_B_GPIO_05	MV	DI, DO	
E5	PM_B_GPIO_08	MV	DI, DO	
E4	PM_B_GPIO_09	MV	DI, DO	
F25	PM_C_GPIO_01	LV	DI, DO	
F26	PM_C_GPIO_02	LV	DI, DO	
F24	PM_C_GPIO_03	LV	DI, DO	
D24	PM_C_GPIO_04	LV	DI, DO	
D2	PM_C_GPIO_05	MV	DI, DO	
D28	PM_C_GPIO_06	MV	DI, DO	
C24	PM_C_GPIO_07	MV	DI, DO	
B24	PM_C_GPIO_08	MV	DI, DO	
C29	PM_C_GPIO_09	MV	DI, DO	
C27	PM_B_AMUX2	1.875V max	AI	
B28	PM_B_AMUX4	1.875V max	AI	
GND1	GND1	–	–	
GND2	GND2	–	–	
GND3	GND3	–	–	
GND4	GND4	–	–	
A3	GND	–	–	
A6	GND	–	–	
A9	GND	–	–	
A12	GND	–	–	
A19	GND	–	–	
A20	GND	–	–	
A25	GND	–	–	
A26	GND	–	–	
A27	GND	–	–	
A30	GND	–	–	

Pin	Pin Name	Voltage	Pin Type	Notes
B3	GND	–	–	
B19	GND	–	–	
B25	GND	–	–	
B26	GND	–	–	
B27	GND	–	–	
B30	GND	–	–	
C1	GND	–	–	
C2	GND	–	–	
C3	GND	–	–	
C19	GND	–	–	
C25	GND	–	–	
C30	GND	–	–	
C31	GND	–	–	
C32	GND	–	–	
D3	GND	–	–	
D6	GND	–	–	
D9	GND	–	–	
D12	GND	–	–	
D19	GND	–	–	
D25	GND	–	–	
D27	GND	–	–	
D30	GND	–	–	
D31	GND	–	–	
D32	GND	–	–	
E12	GND	–	–	
E14	GND	–	–	
E16	GND	–	–	
E18	GND	–	–	
E20	GND	–	–	
E27	GND	–	–	
E29	GND	–	–	
E30	GND	–	–	
E31	GND	–	–	
E32	GND	–	–	
F3	GND	–	–	
F6	GND	–	–	
F11	GND	–	–	
F13	GND	–	–	
F15	GND	–	–	
F17	GND	–	–	
F19	GND	–	–	

Pin	Pin Name	Voltage	Pin Type	Notes
F21	GND	–	–	
F22	GND	–	–	
F27	GND	–	–	
F28	GND	–	–	
F29	GND	–	–	
F30	GND	–	–	
F31	GND	–	–	
F32	GND	–	–	
G22	GND	–	–	
G23	GND	–	–	
G24	GND	–	–	
G25	GND	–	–	
G26	GND	–	–	
G27	GND	–	–	
G28	GND	–	–	
G29	GND	–	–	
J3	GND	–	–	
J6	GND	–	–	
J32	GND	–	–	
K22	GND	–	–	
K23	GND	–	–	
K24	GND	–	–	
K25	GND	–	–	
K26	GND	–	–	
K27	GND	–	–	
K28	GND	–	–	
K30	GND	–	–	
L2	GND	–	–	
L21	GND	–	–	
L25	GND	–	–	
L26	GND	–	–	
L27	GND	–	–	
L28	GND	–	–	
L29	GND	–	–	
L30	GND	–	–	
M21	GND	–	–	
M25	GND	–	–	
M26	GND	–	–	
M27	GND	–	–	
M28	GND	–	–	
M29	GND	–	–	

Pin	Pin Name	Voltage	Pin Type	Notes
M30	GND	–	–	
N3	GND	–	–	
N21	GND	–	–	
N25	GND	–	–	
N26	GND	–	–	
N27	GND	–	–	
N28	GND	–	–	
N29	GND	–	–	
N30	GND	–	–	
P21	GND	–	–	
P22	GND	–	–	
P23	GND	–	–	
P24	GND	–	–	
P25	GND	–	–	
P26	GND	–	–	
P27	GND	–	–	
P28	GND	–	–	
P29	GND	–	–	
R21	GND	–	–	
R28	GND	–	–	
T6	GND	–	–	
T31	GND	–	–	
T32	GND	–	–	
U1	GND	–	–	
U2	GND	–	–	
U6	GND	–	–	
V1	GND	–	–	
V2	GND	–	–	
V5	GND	–	–	
V6	GND	–	–	
W3	GND	–	–	
W5	GND	–	–	
W22	GND	–	–	
W23	GND	–	–	
W24	GND	–	–	
W25	GND	–	–	
W27	GND	–	–	
W28	GND	–	–	
W29	GND	–	–	
W30	GND	–	–	
Y28	GND	–	–	

Pin	Pin Name	Voltage	Pin Type	Notes
Y29	GND	–	–	
Y30	GND	–	–	
Y31	GND	–	–	
Y32	GND	–	–	
AA28	GND	–	–	
AA29	GND	–	–	
AA30	GND	–	–	
AA31	GND	–	–	
AA32	GND	–	–	
AB20	GND	–	–	
AB21	GND	–	–	
AC9	GND	–	–	
AC20	GND	–	–	
AC21	GND	–	–	
AD9	GND	–	–	
AD20	GND	–	–	
AD21	GND	–	–	
AE1	GND	–	–	
AE2	GND	–	–	
AE3	GND	–	–	
AE21	GND	–	–	
AE31	GND	–	–	
AE32	GND	–	–	
AF3	GND	–	–	
AF4	GND	–	–	
AG3	GND	–	–	
AG4	GND	–	–	
AG6	GND	–	–	
AG9	GND	–	–	
AG12	GND	–	–	
AF26	NC	–	–	
AB24	NC	–	–	
AD22	NC	–	–	
AD23	NC	–	–	
AE22	NC	–	–	
AE23	NC	–	–	
AB26	NC	–	–	
AB27	NC	–	–	
B22	NC	–	–	
C23	NC	–	–	
C22	NC	–	–	

Pin	Pin Name	Voltage	Pin Type	Notes
E23	NC	–	–	
D26	NC	–	–	
T3	NC	–	–	
U3	NC	–	–	
P30	NC	–	–	
R30	NC	–	–	
M2	NC	–	–	
M1	NC	–	–	
N2	NC	–	–	
N1	NC	–	–	
P2	NC	–	–	
P1	NC	–	–	
R2	NC	–	–	
R1	NC	–	–	
T2	NC	–	–	
T1	NC	–	–	
L6	NC	–	–	
L5	NC	–	–	
L3	NC	–	–	
L4	NC	–	–	
M3	NC	–	–	
M4	NC	–	–	
H6	NC	–	–	
H5	NC	–	–	
H4	NC	–	–	
H3	NC	–	–	
H2	NC	–	–	
H1	NC	–	–	
AD13	NC	–	–	
AC13	NC	–	–	
AE4	NC	–	–	
AD4	NC	–	–	
C18	NC	–	–	
D18	NC	–	–	
D15	NC	–	–	
C15	NC	–	–	
B15	NC	–	–	
A15	NC	–	–	
D14	NC	–	–	
C14	NC	–	–	
D13	NC	–	–	

Pin	Pin Name	Voltage	Pin Type	Notes
C13	NC	–	–	
A14	NC	–	–	
B14	NC	–	–	
A13	NC	–	–	
B13	NC	–	–	
AG11	NC	–	–	
AF11	NC	–	–	
AG10	NC	–	–	
AF10	NC	–	–	
Y4	NC	–	–	
AC26	NC	–	–	
AC27	NC	–	–	
R29	NC	–	–	
AB9	NC	–	–	
Y3	NC	–	–	
AA10	NC	–	–	
AB29	NC	–	–	
AD26	NC	–	–	
AB28	NC	–	–	
N5	NC	–	–	
AC17	NC	–	–	
AB17	NC	–	–	
AC18	NC	–	–	
AB18	NC	–	–	
AF17	NC	–	–	
AE15	NC	–	–	
AD15	NC	–	–	
AF15	NC	–	–	
AD14	NC	–	–	
AG15	NC	–	–	
AF14	NC	–	–	
AE30	NC	–	–	

Chapter 3. Electrical Characteristics

3.1. Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in 3.2. Operating conditions.

Table 3-1. Absolute rating condition

Parameter	Min	Max	Units
Input Power Voltage			
USB_VBUS	-0.3	28	V
VBATT	-0.3	6	V
VBATT_VSNS_P, VBATT_VSNS_M, RSENSE_EXT_M, RSENSE_EXT_P	-0.3	6	V

3.2. Operating conditions

The SOM needs to be designed in the operation conditons which is shown as below table.

Table 3-2. Operating conditions

Parameters	Min	Typical	Max	Units
Input Power voltage				
USB_VBUS	+3.6	5	+13.2	V
VBATT	+3.6	3.8	+4.8	V
VBATT_VSNS_P, VBATT_VSNS_M, RSENSE_EXT_M, RSENSE_EXT_P	+3.6	3.8	+4.8	V
Thermal conditions				
Operating temperature	-35	25	75	°C
Storage temperature	-40	-	90	°C

➲ **NOTE**: For the thermal conditons, operating and storage min and max temperatures are only valid when the module is fully tested and approved in the Initial Production stage.

3.3. Output power

The SOM provide power supply for external device, like camera module, SD card, sensor, and so on.

Table 3-3. Output power

Function	Pin	Default voltage (V)	Range (V)	Expected use
VPH_PWR	AB31,AB32, AC30,AC31, AC32,AD30, AD31,AD32	-	3.2~4.75	Primary system supply node
VREG_BOB	C20,C21, D20,D21	3.3	-	Buck-boost output 3.3V@1A (will increase to 3.6V during the bootup of the SOM)
VREG_L16B_1P2	AG30	1.2	1.2~1.3	1.2V~1.3V, 1.2V typ
VREG_L17B_1P8	AE20	1.8	1.8~1.9	1.8V~1.9V, 1.8V typ WCD_VDD_BUCK by default
VREG_L18B_1P8	E24	1.8	1.8~2.0	1.8V~2.0V, 1.8V typ (PX_3) Just used for GPIO pull-up
VREG_L2C_1P8	F23	1.8	1.62~1.98	1.62V~1.98V, 1.8V typ MEMS_DMIC_VDD by default
VREG_L3C_3P0	A21	3	2.7~3.54	2.7V~3.54V, 3V typ Touch screen by default
VREG_L4C_1P8_3P0	A23	1.8	1.62~3.3	1.62V~3.3V, 1.8V typ UIM1 Power Supply
VREG_L2B_3P072	D22	3.072	2.7~3.55	3.072V typ; USB redriver by default
VREG_L7C_3P0	W4	3	3.0~3.54	3.0V~3.54V, 3V typ Sensors by default
VREG_L8C_1P8	D23	1.8	1.62~2	1.62V~2V, 1.8V typ Sensors by default
VREG_L11C_2P8	B23	2.8	1.65~3.54	1.65V~3.54V, 2.8V typ Connectivity by default
VREG_L12C_1P8	E22	1.8	1.62~1.98	1.62V~1.98V, 1.8V typ OLED VDDIO by default
VREG_L13C_3P0	A24	3	2.7~3.54	2.7V~3.54V, 2.8V typ OLED VCI by default
VREG_SYS_1P8	W26	1.8	1.75~1.85	System 1.8 V I/O output Reserved for debug, please leave it floating
VIB_DRV_P	AC29	-	1.504~3.544	Power supply for haptics driver

3.4. Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage. The SOM IO voltage level is the same with VDDPX_3 (default: 1.8V) except the SD card and analog input/output. The I2C, USB, MIPI and UART comply with the standards.

3.4.1. Digital GPIO characteristics

The follow-int table shows the digital GPIO characteristics:

Table 3-4. Digital IO voltage performance

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt	0.7 x VDDPX_3	VDDPX_3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt	-0.3	0.3 x VDDPX_3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

3.4.2. SD card digital I/O characteristics

The SDIO is powered by the VDDPX_2 supply, which has a default voltage of 2.96V.

Table 3-5. SD digital IO voltage performance

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	0.65 * VDDPX_2	-	VDDPX_2 + 0.3	V
VIL	Low-level input voltage	-0.3	-	0.25 * VDDPX_2	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/0.75 x VDDPX_2	-	-/VDDPX_2	V
VOL	Low-level output voltage	0/0	-	0.45/0.125 x VDDPX_2	V

3.5. MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Table 3-6. MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

Table 3-7. MIPI_CSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHY v1.2	None

3.6. USB

The SOM supports USB standards and exceptions.

Table 3-8. USB

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)

3.7. PCIe

The SOM supports PCIe standards and exceptions

Table 3-9. PCIe

Applicable standard	Feature exceptions
PCI Express Specification, Revision 3.0	Link configure capability

3.8. DisplayPort

The SOM supports DisplayPort standards and exceptions

Table 3-10. DP

Applicable standard	Feature exceptions
VESA DisplayPort V1.4	None

3.9. SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Table 3-11. SLIMbus

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

3.10. SDIO

The SOM Supports SD standards and exceptions

Table 3-12. SDIO

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

3.11. I2S

The SOM I2S standards and exceptions:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions.

It supports the following functions:

- Both master and slave mode
- 16, 24, or 32-bit resolution audio samples
- 8, 16, 32, 48, 96 and192 kHz sampling rate in Master mode, and all standard sample rates in slave mode.
- 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s)

Maximum clock frequency supported 12.288 MHz.

An additional Pin can be used for a master clock, supplied by the MSM device, the master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Table 3-13. I2S

Applicable standard	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	None

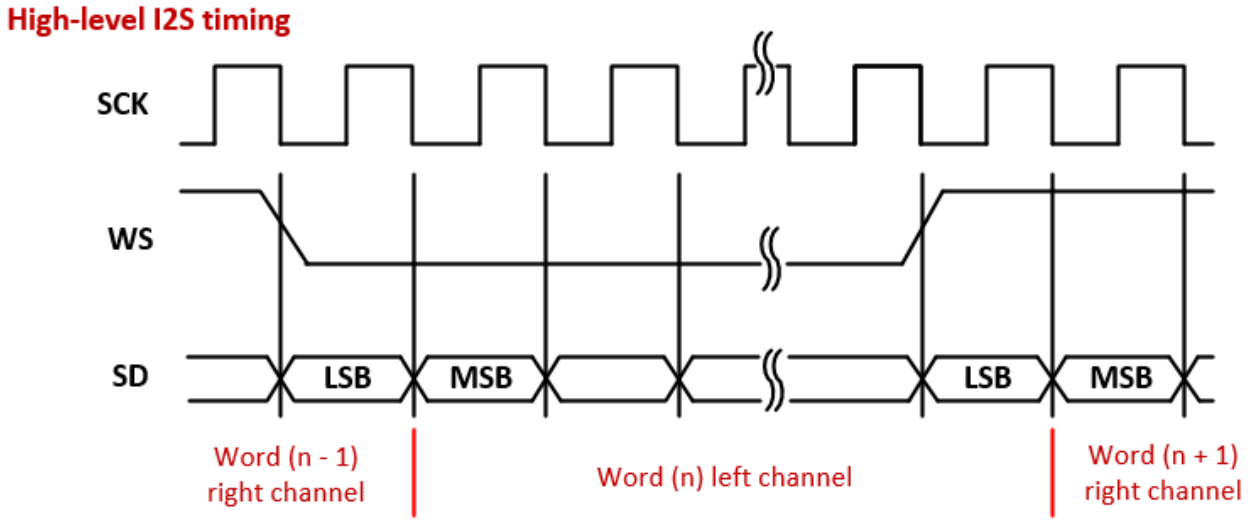

Figure 3-1.I2S Timing Diagram

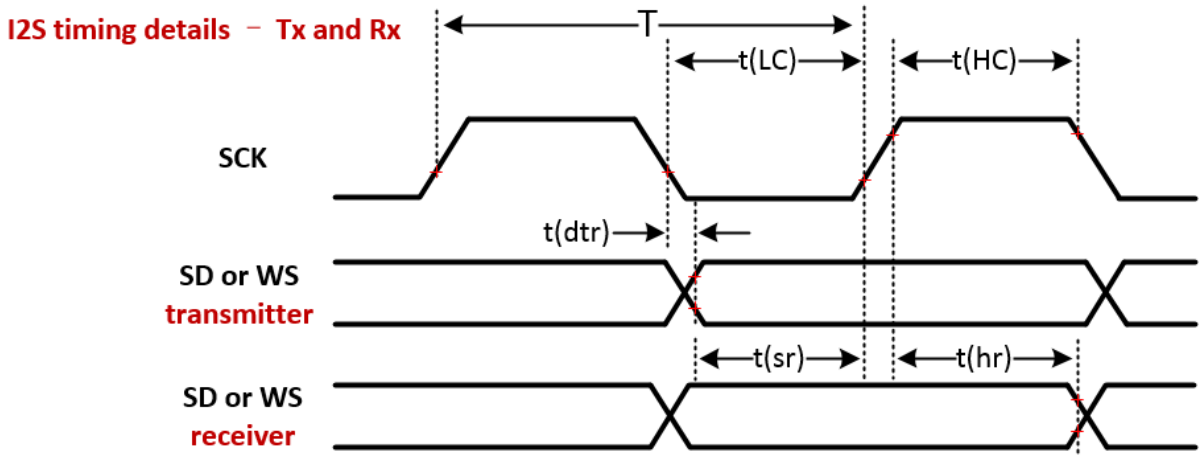

Figure 3-2.I2S Timing Diagram

The word-select signal is a 50% duty cycle signal Data is delayed 1 bit-clock, relative to the word select.

Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.

I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.

The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high.

Table 3-14. I2S Timing

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns

3.12. I2C

The SOM I2C standards and exceptions:

Table 3-15. I2C

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.
I3C Specification, version 1.0	Ternary, multi-master, HCI are not supported.

3.13. SPI

The SOM supports SPI standards as a master only.

3.14. Power consumption

Table 3-16. Full load power consumption

No.	Test Case	Testing Procedure	Test Result	Unit
1	CPU 100% utilization	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power on the DUT and then set CPU utilization to 100%.	1035.03	mA
2	GPU 99% utilization	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power on the DUT and then set GPU utilization to 99%.	1158.72	mA
3	DSP full load	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power on the DUT and then set DSP to full load.	248.12	mA
4	CPU 100% utilization GPU 99% utilization DSP full load	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power on the DUT and then set CPU/GPU/DSP full load.	1958.11	mA

Table 3-17. Sleep mode power consumption

No.	Test Case	Testing Procedure	Test Result	Unit
1	Leakage Current - Power off	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power off the DUT.	0.17	mA
2	Leakage Current - Power on and then off	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power on the DUT and then off.	0.17	mA
3	Sleep (Idle mode)	1. Connect the power monitor DC regulated power supply. 2. Set the power monitor voltage to 4.2V and turn on the monitoring software. 3. Power on the DUT and then set to idle mode.	4.99	mA

3.15. Thermal

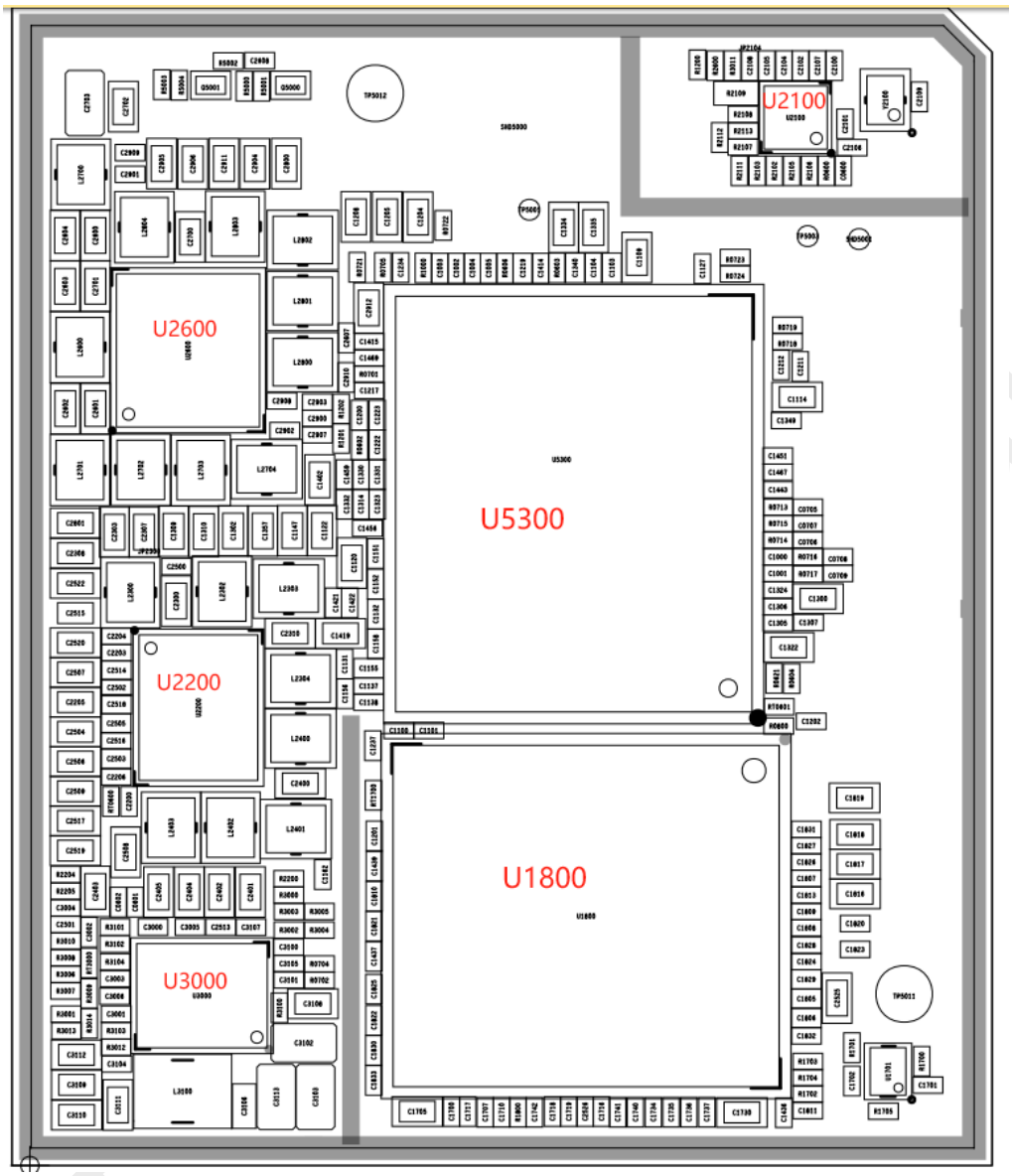

Figure 3-3. Positions of the Measured Components

Test Procedures:

Step 1. Set the temperature of the test chamber to 25°C.

Step 2. Set the power supply of IO to 12V and SOM to 4.2V.

Step 3. Enter the performance mode.

- CPU full load by GPU_Gflops.apk.
- GPU full load by GPU_Gflops.apk.
- DSP full load by Snpebm.

Step 4. Test for 1 hour.

Table 3-18. Thermal test result of measured components (CPU full load)

Test Location (Chip Model)	Temperature (Max)	ΔT
Environment temperature	22.58	0.00
U5300	88.40	65.82
U1800	66.60	44.02
U2100	59.20	36.62
U2600	64.50	41.92
U2200	65.30	42.72
U3000	59.20	36.62

Chapter 4. Packaging

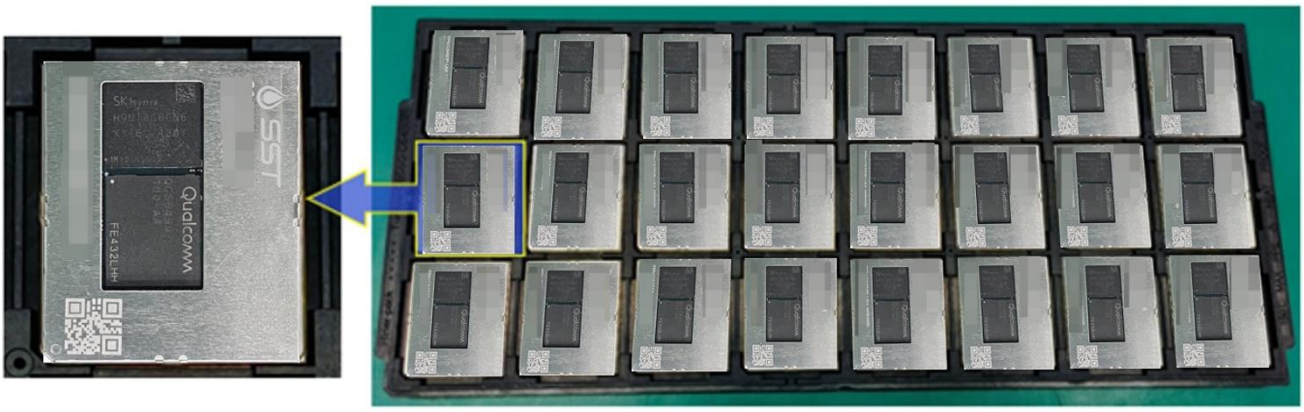

Figure 4-1. Tray Packaging

➲ **NOTES:**

- Place the tray on the workbench with the outer diagonal corner in the bottom left position, as shown in Figure 4-1.
- Align the SOM shield cover diagonal 1PIN marking with the corresponding slot on the tray.
- The tray dimensions are 322.6mm x 136mm x 7.62mm with 24 positions.
- Pay attention to ensure the correct placement of the SOM 1PIN location and perform visual inspection and barcode confirmation.
- After each tray is loaded, scan the QR code on the bottom right corner to confirm the correct positioning.
- Refer to Figure 4-2 for stacking of trays.

Figure 4-2. Stacking of Trays & Carton Packaging

➲ **NOTES:**

- Each tray can accommodate 24 SOMs.
- The trays are stacked in 10 layers, with each layer holding SOMs, resulting in a total of 240 (24 * 10) SOMs per stack.
- An empty tray is placed on the top layer, so each stack consists of 11 trays.
- Each stack includes one desiccant.
- One humidity-sensitive indicator card is placed on the top of each stack.
- Each stack is sealed in an aluminum vacuum bag.
- Two vacuum bags are packed together in one cardboard box.
- MPQ (Minimum Pack Quantity): Each cardboard box can hold a total of 480 (240 * 2) SOMs.

Table 4-1. BOM list of packaging

Item	Description	Dimensions (mm)	Material	Q'ty
①	Carton	415*220*210	230/180/120/180/230-BC	1
②	EPE inner box	400*210*170	20kg/m³, antistatic EPE	1
③	Plastic tray	322.6x136x7.62	PPE (Black)	22
④	Foil bag	500*300	Composite of aluminum foil (PET), PE and film	2
⑤	Activated Clay	40g	N/A	4
⑥	Pearl cotton partition	400*210*20	20kg/m³, antistatic EPE	1
⑦	Wet sensitive identification card	77*51	Paper card	2
⑧	Label	100*100	80g coated paper	1

Refer to Figure 4-3 for the SQC6490 SOM label.

Label Information			
Vendor		Customer	
Product Name		Model	
Brand		SPN	
Order No.		Part No.	
MFG Date		Carton No.	
Made in		QTY	
G.W.		N.W.	
OQC		Remark	

Figure 4-3.SQC6490 SOM Label

Appendix 1. Notices

SST may have patents or pending patent programs covering subject matter described in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries to service@sapphirestreamtech.com.

SST PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some jurisdictions do not allow disclaimer of express or implied warranties in certain transactions; therefore, this statement may not apply to you.

Changes are made periodically to the information herein; these changes will be incorporated in new editions of the publication. To provide better service, SST reserves the right to improve and/or modify the products and software programs described in the manuals, and the content of the manual, at any time without additional notice.

The software interface and function and hardware configuration described in the manuals included with your development board or system on module might not match exactly the actual configuration of that you have purchased. For the configuration of the product, refer to the related contract (if any) or product packing list, or consult the distributor for the product sales. SST may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation to you.

The products described in this document are not intended for use in implantation or other life support applications where malfunction may result in injury or death to persons. The information contained in this document does not affect or change SST product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of SST or third parties. All information contained in this document was obtained in specific environments and is presented as an illustration. The result obtained in other operating environments may vary.

The information of this document should not be as any invitation for offer or any advice to the visitors. Please consult the professional comments from the sales consultant prior to do any actions of investment or purchase.

SST may use or distribute any of the information you supply in any way it believes appropriate without incurring any obligation to you.

Any references in this publication to non-SST websites are provided for convenience only and do not in any manner serve as an endorsement of those websites. The materials at those websites are not part of the materials for this SST product, and use of those websites is at your own risk. SST shall not be responsible for the content of the third party.

Any performance data contained herein was determined in a controlled environment. Therefore, the result obtained in other operating environments may vary significantly. Some measurements may have been made on development-level systems and there is no guarantee that these measurements will be the same on generally available systems. Furthermore, some measurements may have been estimated through extrapolation. Actual results may vary. Users of this document should verify the applicable data for their specific environment.

E-mail messages sent to SST via the Internet are not guaranteed to be completely secure. SST shall not be liable for any loss incurred by the surfer when transmitting any information over the Internet or for any loss incurred by SST when sending any information over the Internet at your request.

SST has all rights under other relevant exemptions provided by laws and regulations, and SST's failure to claim or delay in claiming such rights shall not be deemed to be a waiver of such rights by SST.

SST reserves the right of final interpretation of this document.

Appendix 2. Trademarks

SST is the trademark of Sapphire Stream Technology Co., Ltd. or its associate companies. Intel, Intel SpeedStep, Optane, and Thunderbolt are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Microsoft, Windows, Direct3D, BitLocker, and Cortana are trademarks of the Microsoft group of companies. Mini DisplayPort (mDP), DisplayPort, and VESA are trademarks of the Video Electronics Standards Association. The terms HDMI and HDMI High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries. Wi-Fi, Wi-Fi Alliance, WiGig, and Miracast are registered trademarks of Wi-Fi Alliance. USB-C is a registered trademark of USB Implementers Forum. All other trademarks are the property of their respective owners.